ISSN (Online): 2583-7052

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

Article Title: Design of Low Power Half-Adder & Full-Adder Using Modified Gate Diffusion Input with Zipper Logic

Design of Low Power Half-Adder & Full-Adder Using Modified Gate Diffusion Input with Zipper Logic

P. P. Nagaraja Rao[1], D. Sasikiran[2], K. Bonesh Babu[3], G. Divyasree[4], C. H. Sita Ram Reddy[5], G. Himasagar[6]

[1]Associate Professor, Department of Electronics and Communication Engineering, Sri Venkatesa Perumal College of Engineering and Technology, Puttur, AP, India.
[2,3,4,5,6]UG Students, Department of Electronics and Communication Engineering, Sri Venkatesa Perumal College of Engineering and Technology, Puttur, AP, India.

ABSTRACT

In very large scale integration mainly focusing on three major constraints. That is Time-delay, power consumption, Area of the circuit. In VLSI low power consumption devices has high demand in the market (Mobiles). In VLSI every component work in low supply voltage. Power consumption can be decreased two ways one statically and Dynamic voltage and frequency scaling (DVFS). If circuit complexity increased area will be increasing and power consumption also increases. In cascading circuits one circuit out-put fed into next circuit input. In this situation charge sharing, charge leakage problems exists. To overcome this problems zipper logic is used to the circuit, Zipper logic involves dividing the circuit into smaller sections and synchronizing their operations to minimize power consumption. By activating only necessary parts of the circuit. MGDI is required less number of transistors than compare to CMOS. In this paper half-adder, full adder re-designed using MGDI with ZIPPER logic by using DESIGN SCHEMATIC (for circuit designing) and MICRO-WIND TOOL for simulation in 65nm technology.

Keywords: Complementary metal oxide semiconductor (CMOS), Gate diffusion input (GDI), Modified gate diffusion input (MGDI), Zipper Logic, Very Large Scale Integration (VLSI).

1 Introduction

In Very large scale integration (VLSI) scaling factor is more crucial to design any circuit. Scaling factor refers to the reduction in size of semiconductor devices and interconnects as technology nodes shrink. The scaling factor is typically expressed as a ratio, indicating the reduction in dimensions between different technology nodes.

In Digital circuits Basic digital gates are necessary perform arithmetic and logical operations. Full-Adder is more important to perform additions and multiplication and memory address generation such more applications. If anyone circuit complexity increases then area, delay, power-consumption increase. In electronic devices circuits having many circuits like

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

multiplexers, flip-flops, subtarctor and more circuit may have in any digital devices like (mobile-phones, Laptops). These all circuits complexity increases size of the device is increased and that device would not be dynamic device.
All these portable devices are worked on battery based. These devices power consumption can increases it leads decrease the battery life. From past two decades in VLSI many design methodologies are existed. Such as NOVEL approach. In Novel approach [1][2].

2 Design Techniues

2.1 Pass Transistor Logic (PTL)

Pass-Transistor Logic (PTL) is a type of digital logic family used to implement logic gates and circuits. It utilizes pass transistors as the primary switching elements to perform logic operations. A pass transistor is a type of MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) that can be used to either pass a signal from its input to its output or block the signal, depending on the control signal applied to its gates. Figure1 shows the implementation of AND gate using PTL.
When the control signal is LOW (0), both NMOS and PMOS transistors are off, effectively disconnecting the input and output signals. This state represents logic "0."
When the control signal is HIGH (1), both NMOS and PMOS transistors are turned on, creating a low-resistance path between the input and output. This state represents logic "1." [3].

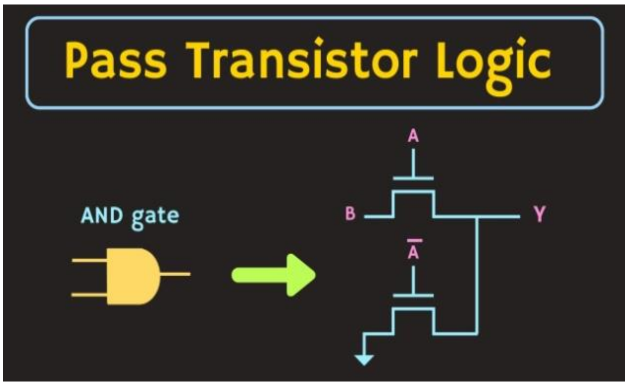

Figure 1: *Implementation of an AND gate using PTL.*

3 Transmission Gate

The transmission gate logic is used to solve the voltage drop problem of the pass transistor logic. This technique uses the complementary properties of NMOS and PMOS transistors. i.e. NMOS devices passes a strong '0' but a weak '1' while PMOS transistors pass a strong '1' but a weak '0'. The transmission gate combines the best of the two devices by placing an NMOS transistor in parallel with a PMOS transistor as shown in Figure below. The control signals to

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

the transmission gate C and —C are complementary to each other. The transmission gate is mainly a bi-directional switch enabled by the gate signal 'C'. When C = 1 both MOSFETs are ON and the signal pass through the gate i.e. A = B if C = 1. Whereas C = 0 makes the MOSFETs cut off creating an open circuit between nodes A and B.Figure2 shows logic symbol of Transmission Gate[4].

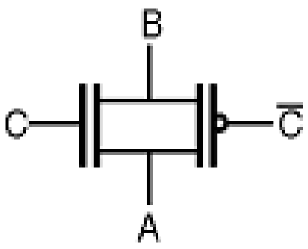

Figure 2: *Transmission Gate*

4 CMOS Technology

CMOS stands for Complementary Metal-Oxide-Semiconductor, and it refers to a common semiconductor technology used in the fabrication of integrated circuits (ICs). CMOS technology relies on the use of both p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs). These transistors are fabricated on a silicon substrate and are arranged in complementary pairs, hence the term "complementary" in CMOS.

CMOS Circuit contain both NMOS and PMOS devices to speed the switching of capacitive loads. It consumes low power and can be operated at high voltages, resulting in improved noise immunity

It consists of two MOSFETs in series in such a way that the P-channel device has its source connected to $+V_{DD}$ (a positive voltage) and the N-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

When input is HIGH, the gate of Q_1 (P-channel) is at 0V relative to the source of Q_1 i.e. V_{GS1} = 0V. Thus, Q_1 is OFF. On the other hand, the gate of Q_2 (N-channel) is at $+V_{DD}$ relative to its source i.e. $V_{GS2} = +V_{DD}$. Thus, Q_2 is ON. This will produce $V_{out} \approx 0$ V.

When input is LOW, the gate of Q_1 (P-channel) is at a negative potential relative to its source while Q_2 has V_{GS} = 0 V. Thus, Q_1 is ON and Q_2 is OFF. This produces output voltage approximately $+V_{DD}$,. Figure3 shows Basic Cmos inverter [5][6].

ISSN (Online): 2583-7052

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

Article Title: **Design of Low Power Half-Adder & Full-Adder Using Modified Gate Diffusion Input with Zipper Logic**

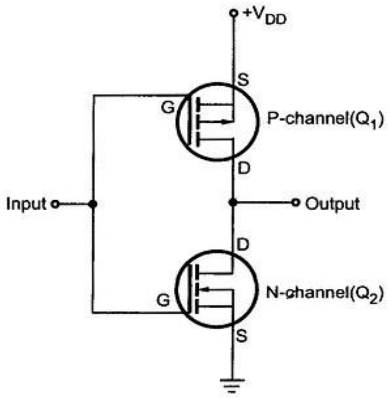

Figure 3: *CMOS Inverter*

5 GDI (Gate Diffusion Input)

The Gate Diffusion Input (GDI) is a method used in digital circuit design to implement logic functions using only one type of transistor (typically nMOS transistors) while maintaining a low power consumption and a compact layout. It is particularly useful in CMOS technology where both nMOS and pMOS transistors are available.

GDI cell is similar to CMOS inverter in cmos p,n type are fixed to the vdd,vss. In GDI p-bulk given to the p-type and n-type bulk given to the n-type. The below Figure4, Table1 shows GDI cell and function [7][8].

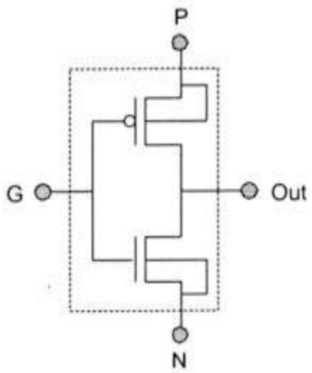

Figure 4: *GDI cell*

Table1: *GDI cell function*

N	P	G	Output	Function
B	0	A	AB	AND
1	B	A	A+B	OR
C	B	A	$\bar{A}$B+AC	MUX
0	1	A	$\bar{A}$	NOT

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

6 Modified Gate Diffusion Input

Modified Gate Diffusion Input (MGDI) is an enhancement of the traditional Gate Diffusion Input (GDI) technique used in digital circuit design. MGDI introduces modifications to the original GDI method to address its limitations and to extend its capabilities. MGDI aims to improve the efficiency, performance, or functionality of GDI-based circuits.
MGDI cell is similar to GDI cell but in MGDI p-bulk given to the vdd and n-bulk given to the vss. Figure 5 shows MGDI cell and Table2 shows MGDI function.
In every cascading circuit have charge leakage and charge sharing problems will exists. However MGDI cell consume more power. To overcome these problems ZIPPER logic is proposed to the MGDI Full Adder [9] [10] [11].

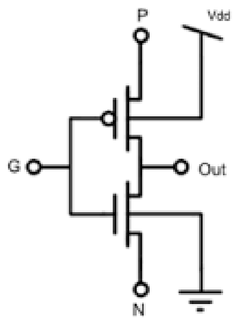

Figure 5: *MGDI Cell*

Table 2: *Function of MGDI Cell*

N	Gnd	P	V_{dd}	G	D	Function
0	0	1	1	A	$\bar{A}$	Inverter
A	A	0	A	B	AB	AND
1	0	A	D	B	A+B	OR
$\bar{A}$	0	A	1	B	$\bar{A}B+\bar{B}A$	XOR
A	0	$\bar{A}$	1	B	$AB+\bar{A}\bar{B}$	XNOR

7 ZIPPER Logic

Zipper logic is a scheme for improving charge leakage and charge sharing problems. Identical to NORA except the clock signals. It receives a slightly different clock signals for the pre-charge (discharge) transistors and for pull down (pull up) transistors. Clock signals which drive pMOS precharge and nMOS discharge transistors, allow the transistors to remain in weak conduction or in cutoff during evaluate phase, thus compensating for charge sharing and charge leakage problems. PMOS pre-charge transistors gates are held at Vdd - |Vtp|. NMOS pre-charge transistors gates are held at Vtn above GND.

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

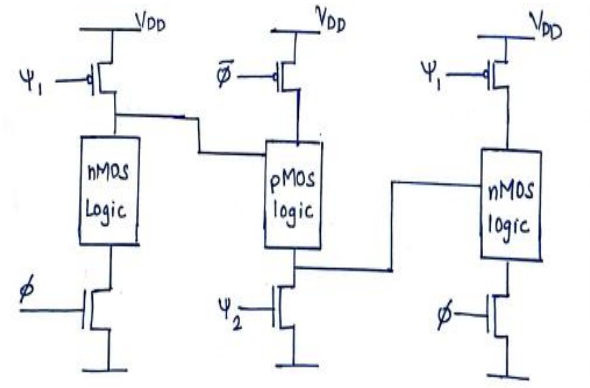

Figure 6: *Basic Block Zipper Logic*

Zipper Logic is a design technique and used to reduce power consumption in digital circuits. Particularly low power devices (like mobiles),it involves dividing the circuit into smaller sections and synchronizing their operations to minimize the power consumption. By activating only necessary parts of the circuit at any given time .This approach helps in reducing Dynamic power consumption. By switching activity. And also improve performance by reducing delays, zipper logic is often used in conjunction with Clock Gating. Figure 6, 7, 8 shows the basic block diagram of Zipper logic, Circuit Diagram of Half-Adder and Circuit Diagram of Full-Adder Respectively.

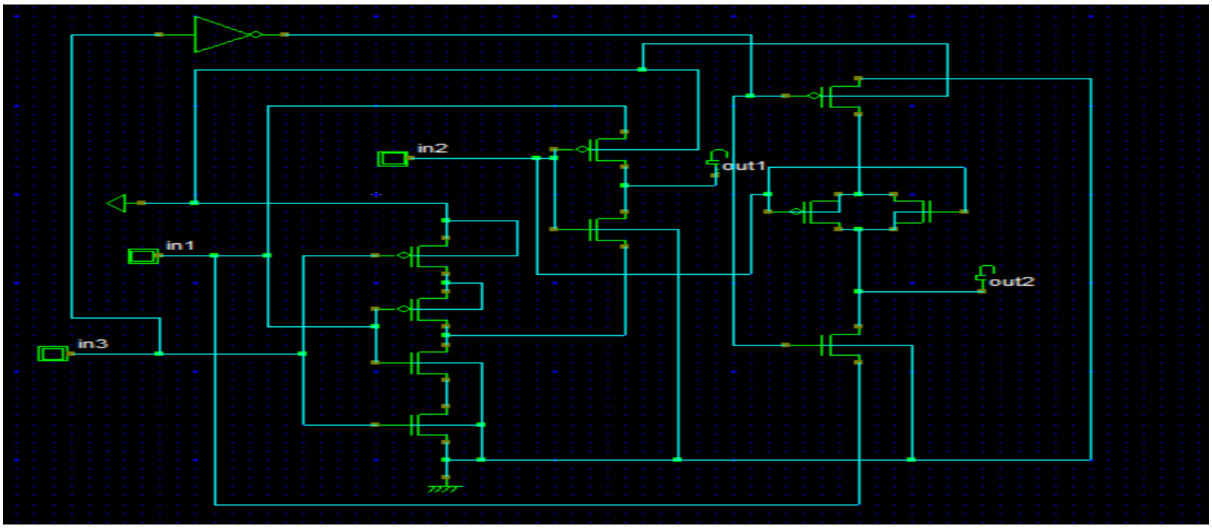

Figure 7: *Half-Adder using MGDI with Zipper logic*

ISSN (Online): 2583-7052

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

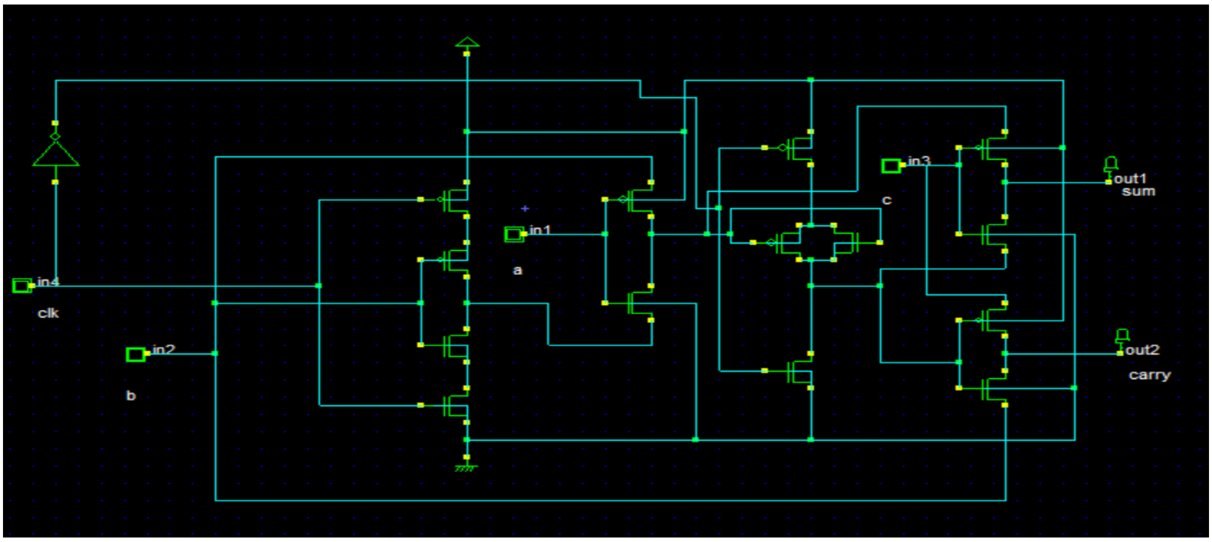

Figure 8: *Full Adder using MGDI with Zipper Logic*

8 Simulation & Results

The Half-Adder, Full-Adder has been designed using the DESIGN SCHEMATIC for circuit design and MICROWIND TOOL for Simulation. Using the GPDK 65 nm technology .The objective of this simulation to decrease power consumption of Half-Adder, Full-Adder. Figure 9, 11 shows the Lambda5 schematic diagram of half-adder, full-adder, Figure10, 12 Shows Power consumption of the Half, Full Adder circuits. Table 3, Figure 13, 14. Represents of Propagation Delay, Power consumption, of MGDI-based with Zipper logic Half-Adder, Full-Adder.

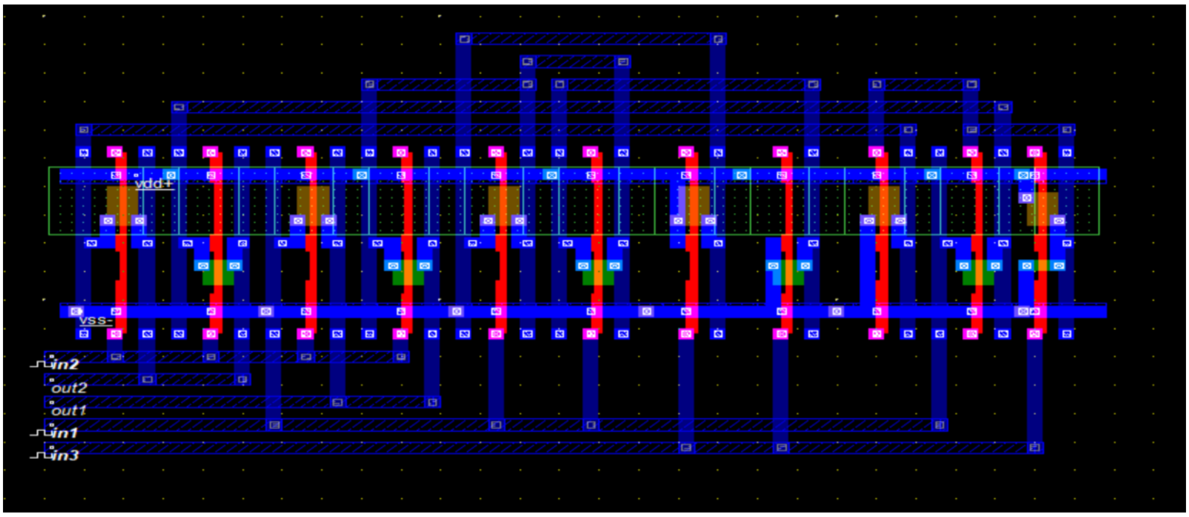

Figure 9: *Layout of Half-Adder using MGDI with Zipper logic*

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

Article Title: **Design of Low Power Half-Adder & Full-Adder Using Modified Gate Diffusion Input with Zipper Logic**

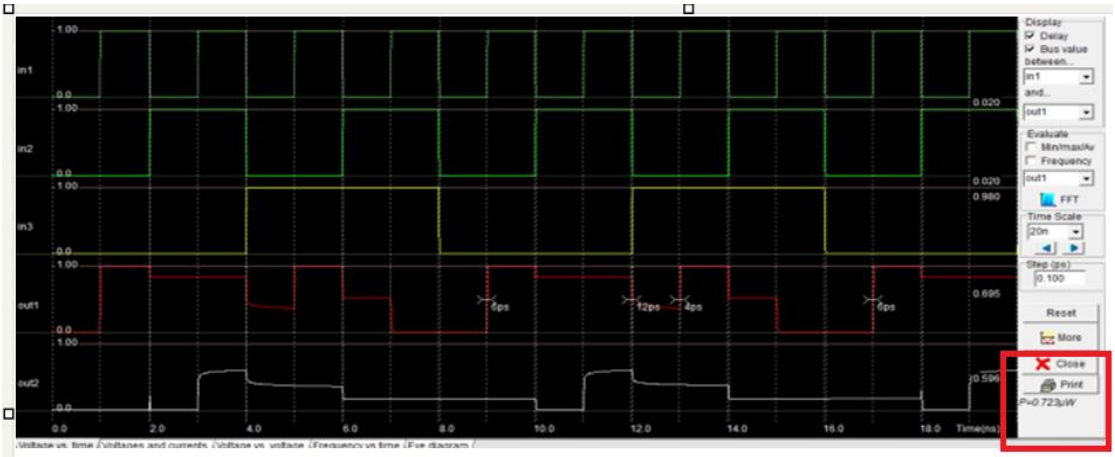

Figure 10: *Power Dissipation of Half-Adder using MGDI with Zipper logic.*

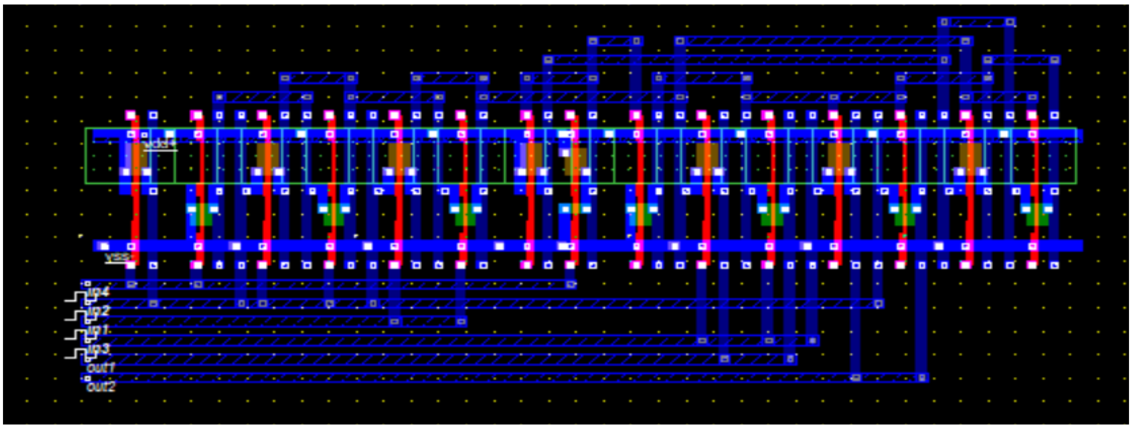

Figure 11: *Layout of Full Adder using MGDI with Zipper Logic*

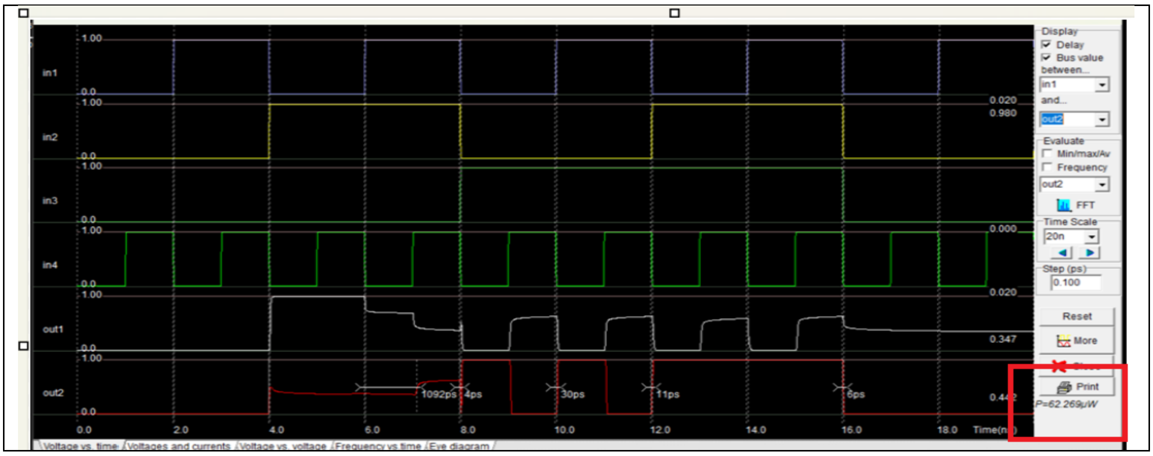

Figure 12: *Power Dissipation of Full Adder using MGDI with Zipper logic.*

ISSN (Online): 2583-7052

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

Article Title: **Design of Low Power Half-Adder & Full-Adder Using Modified Gate Diffusion Input with Zipper Logic**

Table 3: *Power Consumption, Propagation Delay, Transistor Count Half-Adder, Full Adder with Different Technologies*

Digital Circuit	CMOS			MGDI			ZIPPER_LOGIC		
	Propagation Delay(ns)	Power consumption (µW)	Transistor count	Propagation Delay(ns)	Power consumption (µW)	Transistor count	Propagation Delay(ns)	Power consumption (µW)	Transistor count
Half Adder	0.31	139.00	20	0.28	40.19	6	0.26	0.723	10
Full Adder	0.48	189.40	30	0.44	169.30	10	0.42	62.269	14

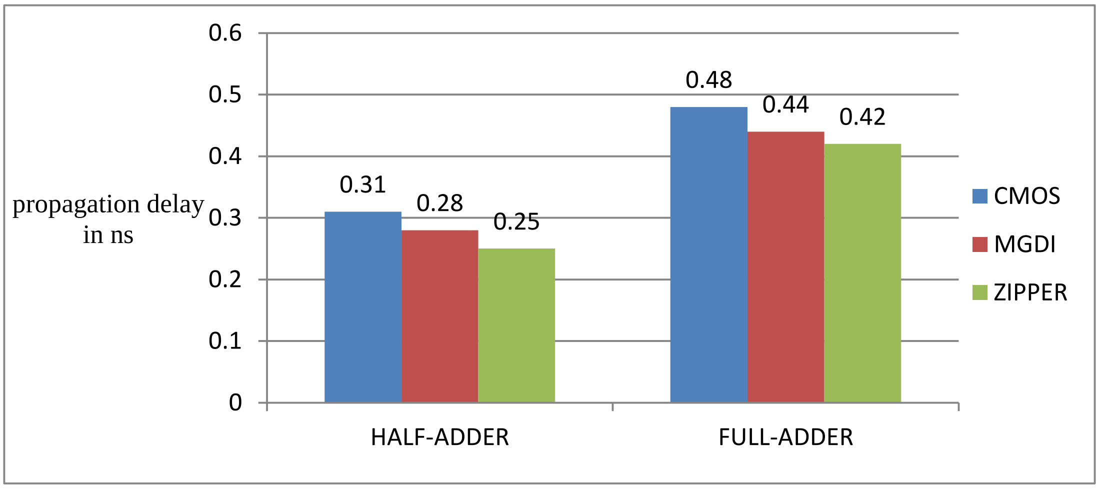

Figure 13: *Bar chart comparison of propagation delay Half-Adder, Full-Adder.*

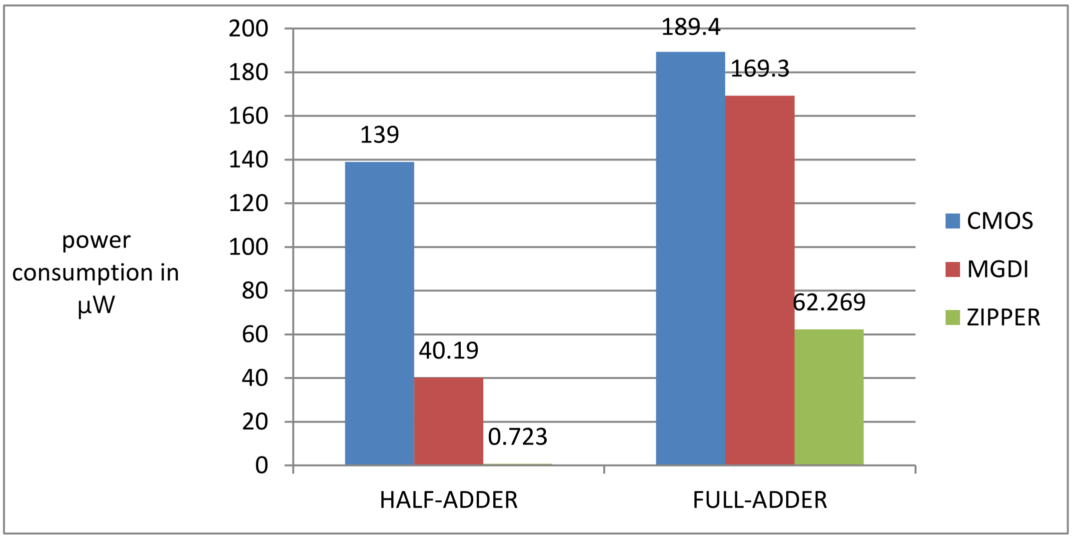

Figure 14: *Bar chart comparison of power consumption for Half-Adder, Full-Adder.*

International Journal of Advanced Trends in Engineering and Management (IJATEM)
pp. 10-20

9 Conclusion

The design and analysis of MGDI-based half adder and full adder circuits using Zipper Logic represent a significant advancement in digital circuit design. Through the utilization of MGDI logic and innovative Zipper Logic techniques, the project has demonstrated the potential to achieve energy-efficient, high-performance digital systems.

The implementation process involved meticulous circuit design, simulation, analysis, and optimization using DSCH and Microwind tools. By carefully selecting gate configurations, transistor sizes, and layout optimizations, the designed circuits exhibited improved power efficiency, speed, and noise immunity compared to conventional CMOS-based designs.

The advantages of MGDI with Zipper Logic, including lower power consumption, higher performance.

References

1. Keivan Navi, Mehrdad Maeen.ed.all, “A Novel low-power full-adder cell for low voltage”. ELSEVIER 2009, Volume 42, Issue 4

2. Ajit Pal, “Low Power VLSI Circuits and System”, New Delhi: Springer; 2015.

3. Bappy Chandra Devanth, Satyendra N Biswas, “An Energy efficient Full-Adder Design Using Pass-Transistor Logic”, International Conference on Innovation in Engineering and Technology 2019

4. Ketkee Kambli, Juili Kolapte.ed.all, “Comparative study of 1-Bit Full Adder using Transmission Gate and Cmos Logic Style”, IJERT ISSN: 2278-0181 2017.

5. Saurabh J Shewale,Sonal A.ed.all, “Design And Analysis of Cmos Full adder”, IJARSCT, Volume 9,Issue1 2021.

6. RashmiKumari, SwapnilRai.ed.all, “Design of Basic Gates Using CMOS”. International Journal of Research (IJR). May 2015; 2(5): 225–226p.

7. Vasanth Kumar,K.P.Vinay.ed.all, “Design implementation of Hybrid Full-Adder using GDI for High Performance Applications”. JCST Issn-1004-9037

8. Dondapati Bindu Sree, K.Rajasekhar, “AHigh-performance Full-Adder Design with Low area Power Delay”. Ijsrst Issn-2395-602X.

9. Shanmuga Priya N, Radha N. “Design and Implementation of Primitive Cells, Fulladder,Fullsubtractor, and Multiplier Using Modified Gate Diffusion input Logic”. ICESC-2020.

10. Khoirom Johnson Singh, Tripurari sharan.ed.all, “High Speed and Low power basic Digital Logic Gates Half-Adder, Full-Adder, using Modified Gate Diffusion Input Technology”. Journal of VLSI Design Tools & Technology. ISSN: 2321-6492, Volume 8,Issue 1.

11. Uma R, Dhavachelvan P. “Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits”. 2nd International Conference on Communication, Computing and Security. 2012