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Leveraging Harbor Seal Whiskers Optimization and Communication Profile Registry for Enhanced 3D NoC Mapping

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ABSTRACT

Conventional application mapping techniques for 3D NoCs frequently face difficulties in simultaneously optimizing power consumption, communication delay, and area efficiency. This paper presents the HaSOA-ADP-3D NoC methodology as a new approach to address these challenges. This paper presents a novel Harbor Seal Whiskers Optimization Algorithm (HaSOA) coupled with a Communication Profile Registry (CPR) for efficient application mapping in 3D NoC architectures (HaSOA-ADP-3D NoC). The proposed methodology aims to optimize communication area, reduce communication delay, and minimize power consumption (ADP). HaSOA inspired by seal whiskers' sensory capabilities, effectively explores the search space, and avoids local optima. CPR captures essential communication characteristics of cores, guiding the optimization process. The proposed HaSOA-ADP-3D NoC method achieves a power consumption of 18.415W, a delay of 12.105 microseconds, and an execution time of 21.115 seconds. Experimental results on standard benchmarks like VOPD and MPEG-4, demonstrate significant improvements in power consumption, communication delay, and overall performance compared to existing methods. The proposed HaSOA-ADP-3D NoC method demonstrates its potential as a valuable tool for developing 3D NoC systems that excel in both performance and energy efficiency.

Keywords: Harbor Seal Whiskers Optimization Algorithm (HaSOA), Communication Profile Registry (CPR), Network-on-Chip (NoC), Power reduction, Delay reduction.

1 Introduction

System-on-Chip (SoC) architectures combine multiple electronic components onto a single chip, resulting in smaller, more energy-efficient devices [1]. However, the proximity of these components leads to communication bottle necks due to limited pathways between processing units [2-5]. Network-on-Chip (NoC) technology addresses this issue by providing a scalable communication infrastructure for SoCs [6-8]. Effective data flow within the NoC necessitates application mapping, which involves strategically assigning tasks to processing elements within the NoC [9]. This placement significantly affects performance metrics such as latency, throughput, area, delay, and power consumption [10]. Traditional application mapping

methods for 3D NoC architectures often face challenges in optimizing all three key parameters like area, delay, and power consumption simultaneously. Recent research has focused on developing application mapping frameworks for 3D NoCs that employ various optimization algorithms to address these challenges. In 2023, Amin, W., et.al, [11] have presented Efficient application mapping approach based on grey wolf optimization for network on chip (GWOA-ADP-3D NoC). But it has high power consumption. In 2023, Habibi, N., et.al, [12] have suggested that the High-performance 3D mesh-based NOC architecture using node-layer clustering using Scalable Universal Matrix Multiplication Algorithm (SUMMA-ADP- 3D NoC). However, it achieves high Delay. In 2023, Bougherara, M., et.al [13] have presented Routing in 3D NoCs using genetic algorithm and particle swarm optimization (GPSOA-ADP-3D NoC). However, it attains high execution time. In 2023, Gopalakrishnan, L. and Ko, S.B., [14] have suggested Mapping 3D NoC architecture design via multi-objective piecewise regressive elitism with spotted hyena optimization. But it suffers from high power consumption. In 2023, Kullu, P. et.al. [15], presented Artificial Bee Colony Based Mapping Method for Three- Dimensional Network-on-Chip. But it leads to high communication delays. This paper introduces the Harbor Seal Whiskers Optimization Algorithm(HaSOA) coupled with a Communication Profile Registry (CPR) to advance application mapping in 3D Networks-on- Chip (NoCs). The proposed HaSOA-ADP-3D NoC methodology addresses critical challenges in optimizing communication area, reducing communication delay, and minimizing power consumption (ADP). The HaSOA inspired by the sensory capabilities of seal whiskers, effectively explores the search space, avoiding local optima. The CPR plays a crucial role by capturing key communication characteristics of cores, which guides the optimization process.

The Key contributions of the proposed HaSOA-ADP-3D NoC methodology include,

- It focuses on three pivotal factors like area, delay, and power consumption for ensuring efficient application mapping in 3D NoC architectures.
- HaSOA exploits the advantages of both mesh and torus topologies, balancing simplicity, regularity, and communication efficiency.
- Experimental results, utilizing standard benchmarks such as VOPD and MPEG-4, indicate substantial improvements in power consumption, communication delay, and overall system performance when compared to existing methods.

The remainder of the manuscript is structured as follows: Section 2 presents power, area, and delay modeling for 3D NoCs. Section 3 details the proposed HaSOA-ADP-3D NoC method. Section 4 evaluates the performance of HaSOA-ADP-3D NoC and presents experimental results. Finally, Section 5 concludes the manuscript.

1.1 Power, Area, and Delay Modeling for 3D NoCs

This section delves into the critical performance metrics of a 3D Network-on-Chip (NoC)

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architecture. The primary objective is to minimize area, delay, and power consumption (ADP). To achieve this, the following aspects will be analyzed:

Power Modeling

The power model determines the total power consumption of a 3D NoC by assessing the energy expenditure of its global links and routers. In Global Link Power modelling, it includes circuit switching, short circuit, and static power. Mathematically represented as equation (1)

$$Power_{GL}=Power_{\text{circuit switching}}+Power_{\text{short circuit}}+Power_{\text{static}} \quad (1)$$

Normally, Vertical switching power depends on TSV capacitance, influenced by substrate permittivity, depth, and oxide/depletion radii. Mathematically represented as equation (2)

$$Power_{Vertical\ Switching}=\frac{2\pi \times \text{substrate permittivity} \times \text{depth}}{1\left[\frac{Depletion\ radii}{Oxide\ radii}\right]} \quad (2)$$

In Router Power, it estimated using a separate power model [17]. Finally Total Power calculation, it considers traffic distribution and communication between processing elements. Mathematically represented as equation (3)

$Power_{Total}$ = Traffic distribution matrix × Communication between processing elements (3)

Area Modeling

For Total Area calculation, it includes switch area, average IP core area, and interconnect area. Mathematically represented as equation (4)

$$A_{Total}=A_{\text{switch}}+A_{\text{average IP core}}+A_{\text{interconnect}} \quad (4)$$

Switch area depends on the number of planes and switch area per plane. Mathematically represented as equation (5)

$$A_{\text{switch}}=\text{Number of planes} \times \text{Area of each switch} \quad (5)$$

Interconnect area for mesh and torus depends on their link counts, determined by network dimensions [17]. Mathematically represented as equation (6)

$$A_{\text{interconnect}}=N_{li}[\text{flitsize}(Wire_{width}+Wire_{Spacing})+Wire_{Spacing}]+Length_{Interconnect} \quad (6)$$

Delay Modeling

The delay of a mesh /torus 3D NoC is calculated using equation (7)

$$Delay_{Total}=A_{HC}\times D_{router}+[A_{HC}\times D_{\text{Horizontal }channel}]+[A_{HC}\times N_{Verticallinks}\times D_{Verticalchannel}]+D_{\text{serialization}} \quad (7)$$

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In this context, D_{router} is the average router delay, $D_{channel}$ is the horizontal/vertical channel delay per hop, $D_{\text{serialization}}$ is the serialization delay, $N_{Verticallinks}$ is the number of vertical links, and $A_{HC}$is the average hop count.

2 Proposed Methodology

This section presents a novel Harbor Seal Whiskers Optimization Algorithm and Communication Profile Registry-based methodology for mapping applications onto 3D NoCs. This methodology effectively explores and exploits the solution space while capturing core communication characteristics.

The initial step characterizes application communication demands by constructing an Application Core Graph (ACG). ACG vertices represent cores, and edges with weights represent communication links and traffic volumes. A Topology Graph (TG) represents the target 3D NoC architecture. To facilitate informed mapping decisions, a Communication Profile Registry (CPR) is created.

In this context, Communication weight$_{uv}$ is the communication weight to neighboring core v, Additionally, the CPR stores information about neighboring cores, including their number and individual communication weights, for grouping cores with high communication demands. After this, Harbor Seal Whiskers Optimization Algorithm (HASOA) for 3D NoC Application Mapping. HASOA is a metaheuristic inspired by seal whiskers, designed to optimizes core mapping in 3D NoCs by efficiently exploring the search space, ensuring computational efficiency, and avoiding local optima. It models seal prey-tracking to optimize core placements. The steps are as follows,

Step 1: Initialization

Initially, initial population of candidate mappings S_M is generate during equation (8)

$$Pop=S_{1,2},\ldots\ldots\ldots\ldots,S_M \tag{8}$$

Where each mapping S_a representing a core placement in the 3D NoC. Then assign cores from the application to nodes in the 3D NoC randomly.

Step 2: Fitness Evaluation

Here, each mapping's fitness based on power consumption, area overhead, and communication delay is evaluated using equation (9)

$$(S_a)=\beta_1\times Power(S_a)+ \beta_2\times Area(S_a)+\beta_3\times Delay(S_a) \tag{9}$$

where $Pow(S_a)$, $Area(S_a)$,and $Delay(S_a)$ are the power, area, and delay of mapping S_a, respectively, and β_1, β_2, and $\beta_3$are weighting factors.

Step 3: Sensing Velocity Calculation

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In this, the sensing velocity for each mapping inspired by seal whiskers' dynamics is evaluated. In this context, V_a is the sensing velocity for each mapping (S_a), Ps_a is the seal's position, Dt is the distance to prey, α is a scaling factor using equation (10)

$$\alpha=2\pi\times\omega\times DisAmp\times OscSD\times Time \quad (10)$$

In this context, is angular frequency, $Dis\ Amp$ is displacement amplitude, $OscSD$ is oscillating sphere diameter.

Step 4: Sensing Velocity Update

In this, the sensing velocity based on the mapping's fitness and its position relative to global and local best solutions is updated [16]. In this context, μ_1, μ_2, and μ_3 are random numbers, $G\ Ps_{Ideal}$ and $L\ Ps_{Ideal,}$ represent global and local best positions, τ is the water flow attack angle, x and y are ellipse axis lengths using equation (11-12)

$$x=0.14\times s(0.92\times\mathbb{N}+1.5\times\pi)+1 \quad (11)$$

$$y=0.067\times s(0.91\times\mathbb{N}+\pi)-0.0041\times\mathbb{N}+0.64 \quad (12)$$

In this context, $\mathbb{N}$ is the number of whisker cross-sections.

Step 5: Position Update

Here the mapping's position based on its calculated sensing velocity is updated.

Step 6: Termination

The HaSOA optimization process continues iteratively until a stopping criterion is met, such as reaching a maximum number of iterations or achieving a satisfactory fitness value. The final mapping configuration with the best fitness value represents the optimal solution for core mapping in the 3D NoC architecture.

3 Results and Discussion

This section evaluates the proposed HaSOA methodology for 3D NoC application mapping (HaSOA-ADP-3D NoC). Simulations were conducted using Python on standard benchmarks (VOPD and MPEG-4) to optimize communication efficiency, minimize power, area, and delay. The simulations were performed on personal computer with an Intel Core i5 CPU at 2.50 GHz, 8GB of RAM, and Windows 7. The HaSOA-ADP-3D NoC method was compared with existing methods like grey wolf optimization (GWOA-ADP-3D NoC) [11], Scalable Universal Matrix. Multiplication Algorithm (SUMMA-ADP-3D NoC) [12], genetic algorithm and particle swarm optimization (GPSOA-ADP-3D NoC) [13]. Results are presented in Figures 1-3.

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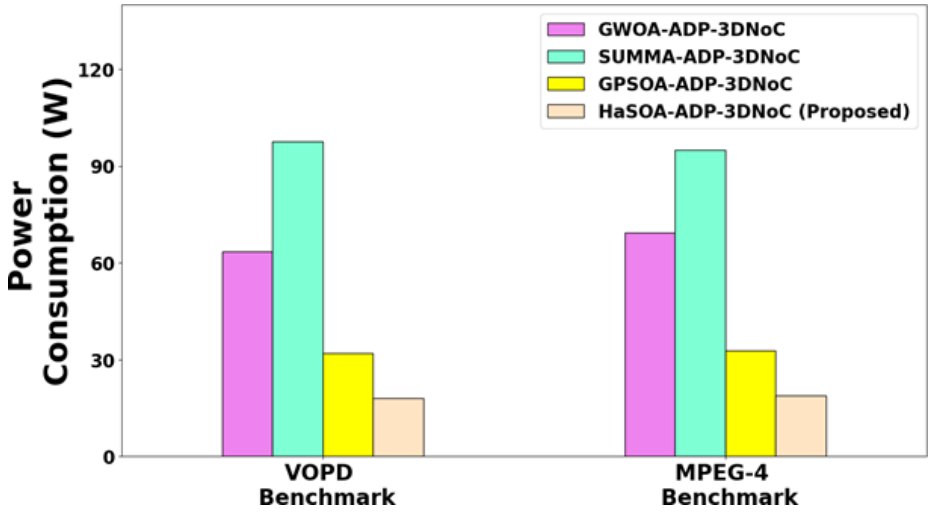

Figure 1: *Power consumption comparison of HSOA-ADP-3D NoC, GWOA-ADP-3D NoC, SUMMA-ADP-3D NoC, and GPSOA-ADP-3D NoC for VOPD and MPEG-4 benchmarks*

Figure 1 demonstrates the significant power savings achieved by the proposed HaSOA-ADP-3D NoC method compared to existing methods like GWOA-ADP-3D NoC, SUMMA-ADP-3D NoC, GPSOA-ADP-3D NoC for both VOPD and MPEG-4 benchmarks. For the VOPD benchmark, proposed HaSOA-ADP-3D NoC method consumes 71.7%, 81.59% and 43.65% less power compared to GWOA-ADP-3D NoC, SUMMA-ADP-3D NoC, GPSOA-ADP-3D NoC respectively. Similarly impressive results are observed for the MPEG-4 benchmark, where the proposed HaSOA-ADP-3D NoC method achieves reductions of 72.8%, 80.14% and 42.42% compared to the existing methods respectively. This shows, HaSOA-ADP-3D NoC significantly reduces power consumption, leading to improved energy efficiency in 3D NoC systems. Figure 2 demonstrates the delay of the proposed HaSOA-ADP-3D NoC method compared to existing methods like GWOA-ADP-3D NoC, SUMMA-ADP-3D NoC, GPSOA-ADP-3D NoC for both VOPD and MPEG-4 benchmarks. HaSOA-ADP-3D NoC significantly reduces delay, outperforming existing methods by 69.93%, 80.507% and 72.32% for VOPD, and by 64.34%, 76.94% and 44.17% for MPEG-4. This demonstrates HaSOA-ADP-3D NoC's effectiveness in improving communication efficiency in 3D NoC architectures.

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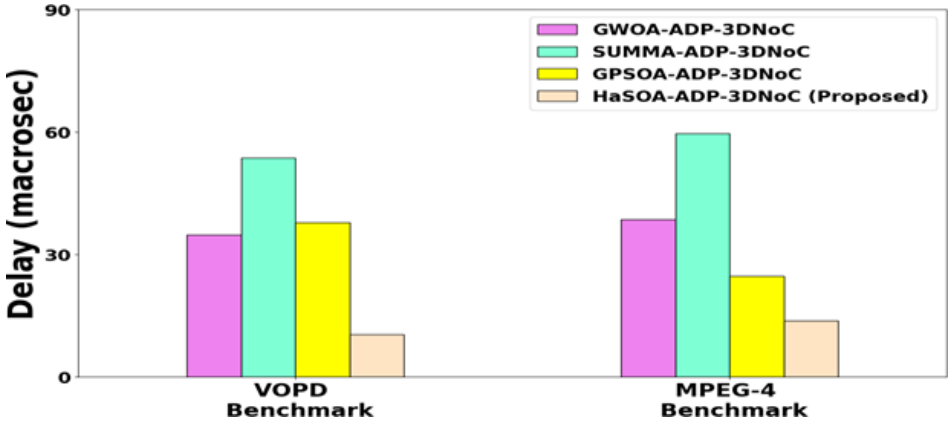

Figure 2: *Delay of HSOA-ADP-3D NoC, GWOA-ADP-3D NoC, SUMMA-ADP-3D NoC, and GPSOA-ADP-3D NoC for VOPD and MPEG-4 benchmarks*

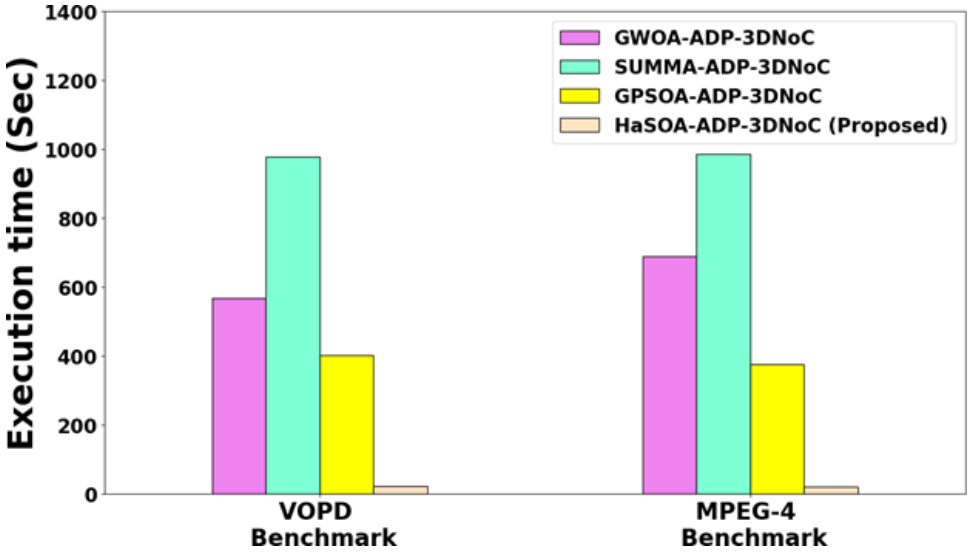

Figure 3: *Execution time of HSOA-ADP-3D NoC, GWOA-ADP-3D NoC, SUMMA-ADP- 3D NoC, and GPSOA-ADP-3D NoC for VOPD and MPEG-4 benchmarks*

Figure 3 demonstrates the Execution time of the proposed HaSOA-ADP-3D NoC method comparedtoexistingmethodslikeGWOA-ADP-3D NoC, SUMMA-ADP-3D NoC, GPSOA-ADP- 3D NoC for both VOPD and MPEG-4 benchmarks. The proposed HaSOA-ADP-3D NoC method attained 96.22%, 97.807% and 94.65% lower Execution time for VOPD benchmark and 96.98%, 97.89% and 94.48% lower Execution time for MPEG-4 benchmark compared with existing methods respectively.

4 Conclusion

The proposed HaSOA-ADP-3D NoC methodology provides a promising approach for efficient

application mapping in 3D NoC architectures. By leveraging HaSOA's exploration capabilities and CPR's core communication characterization, the methodology effectively optimizes power consumption, communication delay, and overall performance. Experimental results validate the superiority of HaSOA-ADP-3D NoC over existing methods. The proposed HaSOA-ADP-3D NoC method attained 72.25%, 80.86% and 43.039% low power consumption, 67.13%, 78.72% and 58.25% lower Delay and 96.604%, 97.85% and 94.57% lower Execution time compared with existing methods like GWOA-ADP-3D NoC, SUMMA-ADP-3D NoC, GPSOA-ADP-3D NoC respectively. Future research will investigate the integration of deep learning techniques to dynamically adjust the exploration-exploitation balance within the HaSOA-ADP-3D NoC framework, potentially improving its adaptability to real-world NoC designs.

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