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ABSTRACT

This project deals with the implementation of inverter which is based on asymmetrical cascaded of bridge producing a 63 level output. With the help of this topology we come to know that a total of 124 switches either MOSFET switches are used. This results in usage of heavy components so to reduce it we decrease the number of DC sources to 5 which now currently as 31 DC sources by binary code we reduce it to 5 DC source and 5 switches [1]. Further the 5 DC sources are reduced to one by implying the fly back converter. This on the whole receives up to 2% of total harmonic distortion (THD).

Keywords: Multilevel Inverter, Flyback Converter, 63-Level Topology, THD.

1 Introduction

Nowadays, electric power generation through PV systems has emerged as an alternative to conventional power generating systems due to simple maintenance, eco-friendly nature, low noise and abundant availability [2]. Extracting maximum power and inverting the output power of the PV system into useful AC to feed the utility are the tedious task associated with solar power generation. To feed the utility grid DC power generated from the PV array has to be inverted into AC power. The conversion circuit includes a dc-dc power converter and Multi-Level Inverter (MLI). Multi-level inverters (MLIs) are the most popular means for voltage conversion from DC to AC power, and are used in fuel cell and photo-voltaic (PV) based sustainable or renewable energy systems (RES). In this project a Novel PV fed Fly back converter based MLI is introduced for grid utility applications[3]. The generated power from PV is fed to the load power network through an inverter. For high power applications it is necessary to transform the generated DC into AC. For this conversion, traditional two level inverter is not sufficient due to harmonics and switching losses. Hence, a novel 31level based MLI is introduced for domestic applications and elimination of harmonic distortion and its effects.



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2 Block Diagram

In this proposed system, the output from the solar systems are enhanced with the aid of a Fly back converter and is regulated by PI controller. Further, the constant DC supply achieved is supplied to the the utility grid of the proposed converter with unity power factor, using a 63-level MLI (Multilevel Inverter) [4]. The proposed topology generates maximum 63-level output voltage with asymmetric DC sources with an H-bridge. This reduces the overall components count, cost and size of the system. Rather than the many advantages of MLIs, reliability issues play a significant role due to higher components count to reduce THD [5]. Several parameters are analysed for the 63-level MLIs such as total standing voltage (TSV), cost function (CF) and power loss. The obtained total harmonic distortion (THD) is under the IEEE standards. This proposed topology is simulated in MATLAB/Simulink and verified experimentally with a hardware prototype under various conditions [6].

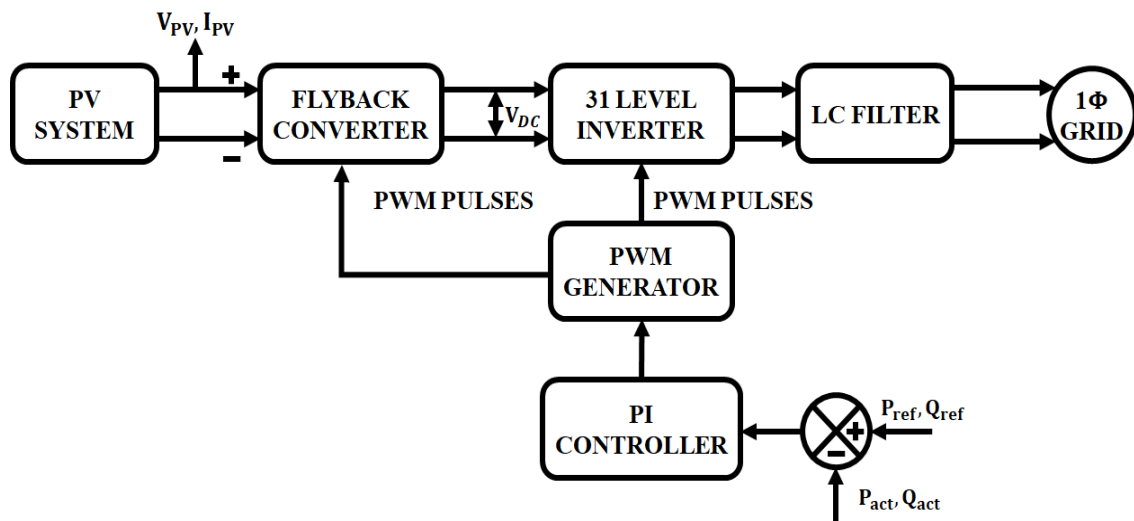


Figure 1: Block Diagram

3 Design Calculations of Fly Back Converter

Generally, the topology of fly back converter has a coupled inductor in which the primary side is provided with a PWM switch and the secondary side with a diode. Figure 2 depicts a general fly back converter. A continuous or variable dc input is supplied to the fly back converter. In accordance with the winding link of coupled inductor, the direction of diode can be changed. The secondary side windings can be increased corresponding to the uses. The circuit should be operated with a continuous dc source in order to reduce its complexity. The switch used should be a device having high switching frequency (“ Q_1 ”). To achieve rapid dynamic control over duty ratio, MOSFET is used. The coupled inductor is used to isolate voltage [7].



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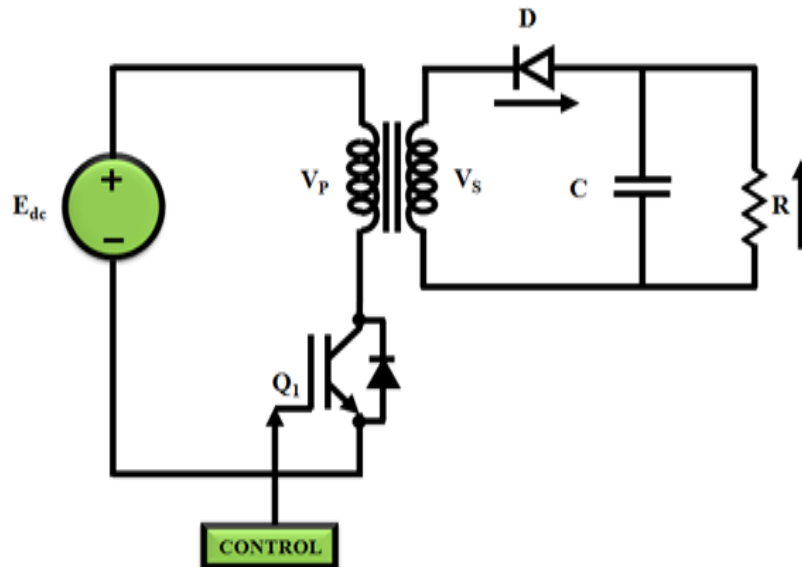


Figure 2: *Fly back Converter*

The figure highlights a flying capacitor multilevel fly back converter which uses switched-diode-capacitor (SDC) stage in order to get higher conversion ratio above 10:1 with efficiency greater than 95%. Red outline shows the single SDC stage. The volume of the inductor, switch stress and capacitor are reduced by the cascaded output stages of SDC [8].

Various output stages are cascaded in conventional boost converter, in which the MLFC (Multilevel Flying Capacitor) converter is generally employed in buck, boost inverter uses. The additional three stages of SDC (flying capacitors Cf1 to Cf3) reduces the output by a factor of five which is liable by each stage. The voltage $(k \cdot V_{out}) / (N-1)$ is equalized by the flying capacitors during the operation of steady-state, where k denotes the interest stage and N denotes level of converters. The necessary voltage rating of the components and their volume can be reduced by dividing the electronic system stress among multiple stages [9].

The inductor will be charged by making the switches S1-S4 ON. When S1 is turned OFF, energy is released by L with the help of Df1 to stage 1 and with S2-S4 to earth. Energy is released by the inductor in order to charge Cf2 after recharging by making the current to pass via S1, Cf1, Df2 and S3-S4 to ground. When all the switches are ON, the inductor will be charged then and this action replicates to charge every stage using inductance energy and capacitor of prior stage.

The flying capacitor multilevel fly back converter (FCMFC) consists of M number of fly back converters which are serially connected at the output, which has N number of stages of voltage ($N-1$ SDC stages) in every fly back [10]. Every fly back transformer consists of n number of turn's ratio. While flyback converters offer many advantages, they also have some drawbacks, such as lower efficiency compared to other converter topologies like the forward converter.



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Additionally, they can produce electromagnetic interference (EMI) due to their switching operation, which may require additional filtering components [11]. Overall, flyback converters are a versatile and widely used power conversion solution, particularly in applications where isolation and regulation are essential.

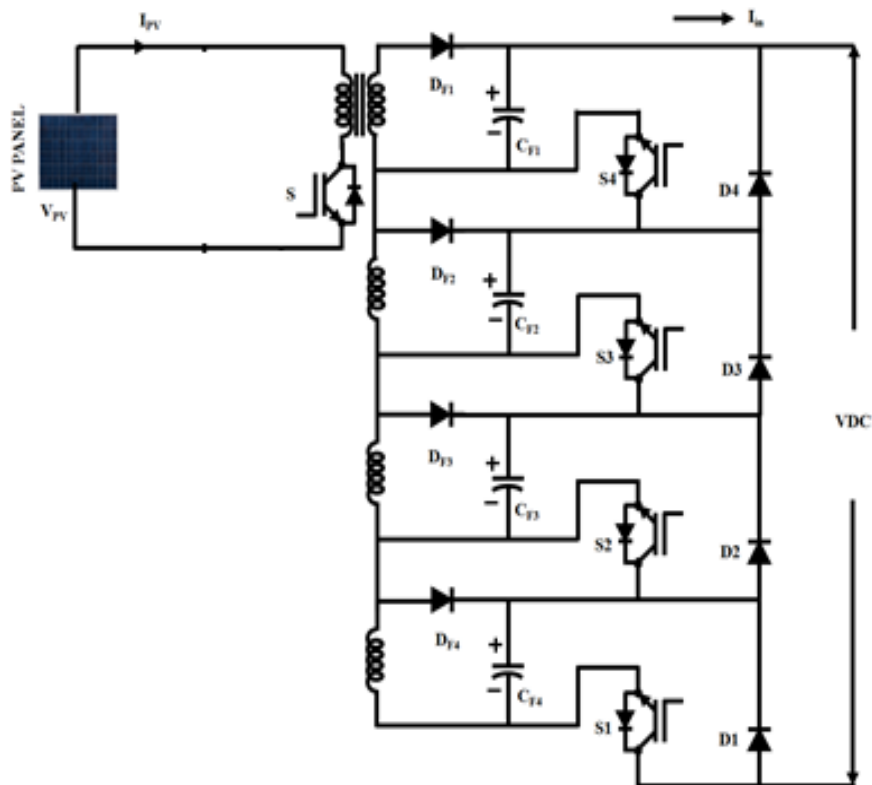


Figure 3: Flyback converter topology

4 63 Level Topology

The output voltage is generated using a multi carrier pulse width modulation approach with 63 levels. The switches S1, S2, S3, and S4 receive these PWM signals [12]. The carrier triangle signal is compared to the two sinusoidal signals with 180 degree displacements after that. Because the PWM pulses have a dead band, this prevents shoot through between the two devices. The single phase inverter circuit switches H1, H2, H3, and H4 receive these PWM pulses. The switching component in this case is a MOSFET, which is less expensive than an IGBT. PIC, or peripheral interface controller, is the processor that is used in here [13].



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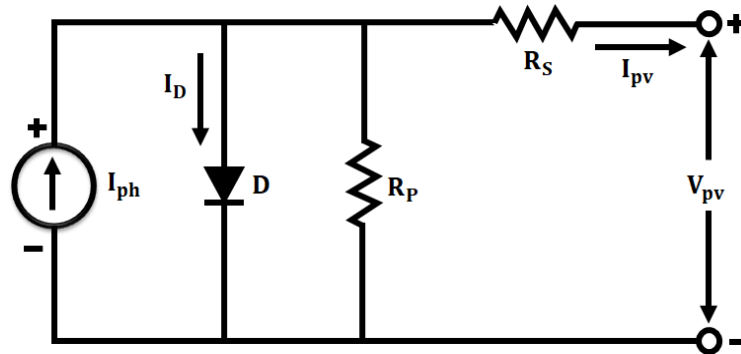


Figure 4: Equivalent circuit of solar PV

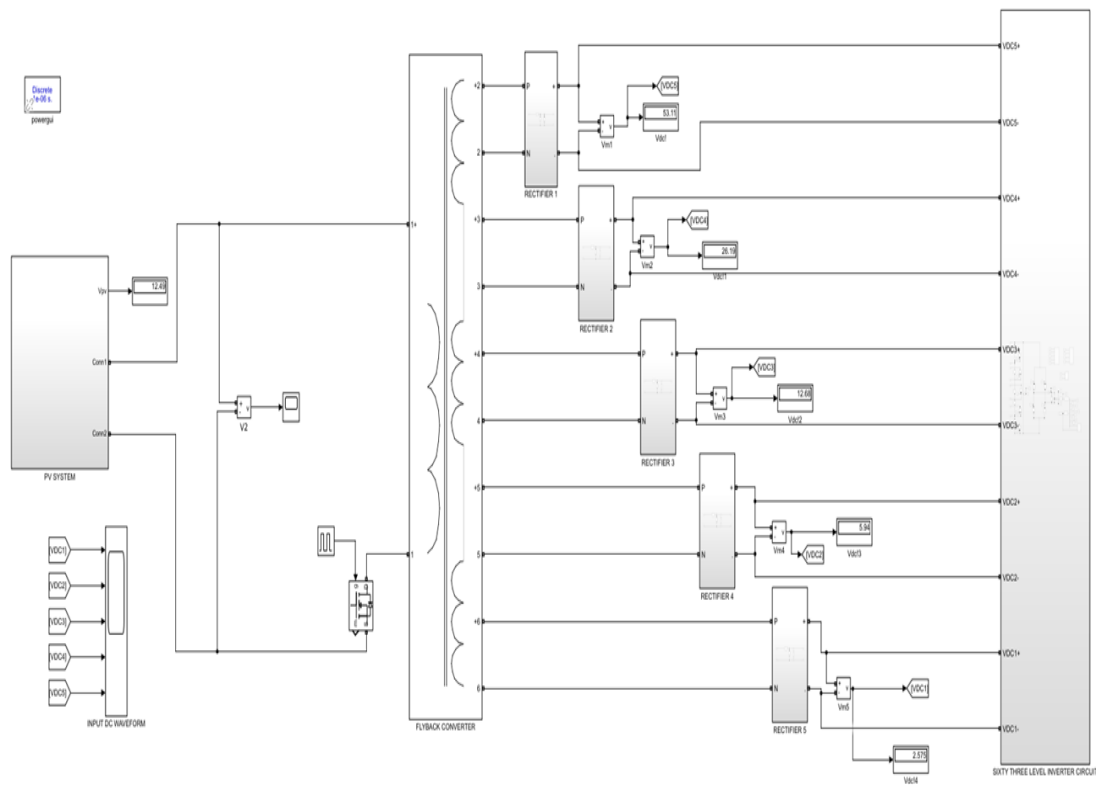


Figure 5: Simulation details for multilevel inverter

5 Simulation using Simulink

Building the system model is then accomplished through a series of steps: The necessary blocks are gathered from the library browser and placed in the model window. The parameters of the blocks are then modified to correspond with the system we are modeling. Finally, the blocks are connected with lines to complete the model. Each of these steps will be explained in detail

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using our example system. Once a system is built, simulations are run to analyze its behaviour [14].

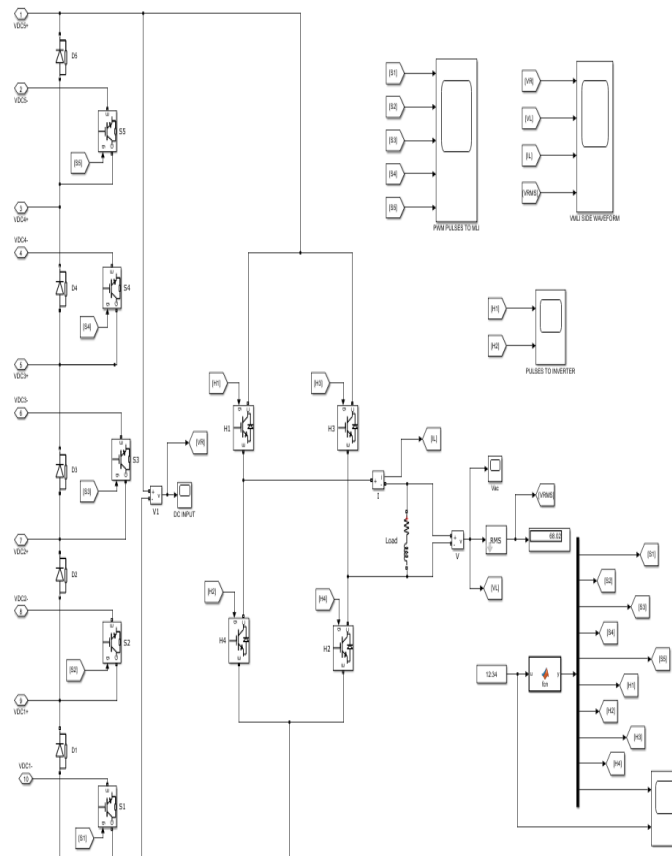


Figure 6: Simulation details for 63 Level Inverter Circuit

The results can be verified using MATLAB/SIMULINK. MATLAB is used for computing, visualizing and programming very easily using certain notation of mathematics. Signal analysis can be performed by MATLAB. The simulation starts by starting the MATLAB, where the Simulink library is present, click it and using browser menu select ‘model’ and thus the results of our model are present there in that particular section. In order to use the SIMULINK browser we need to use the MATLAB running in the background. For control purposes the analysis of simulation is performed using the MATLAB/SIMULINK. Most people use MATLAB as it helps them to try different ideas into simulation where it can be tested with various parameters and different values for different devices.



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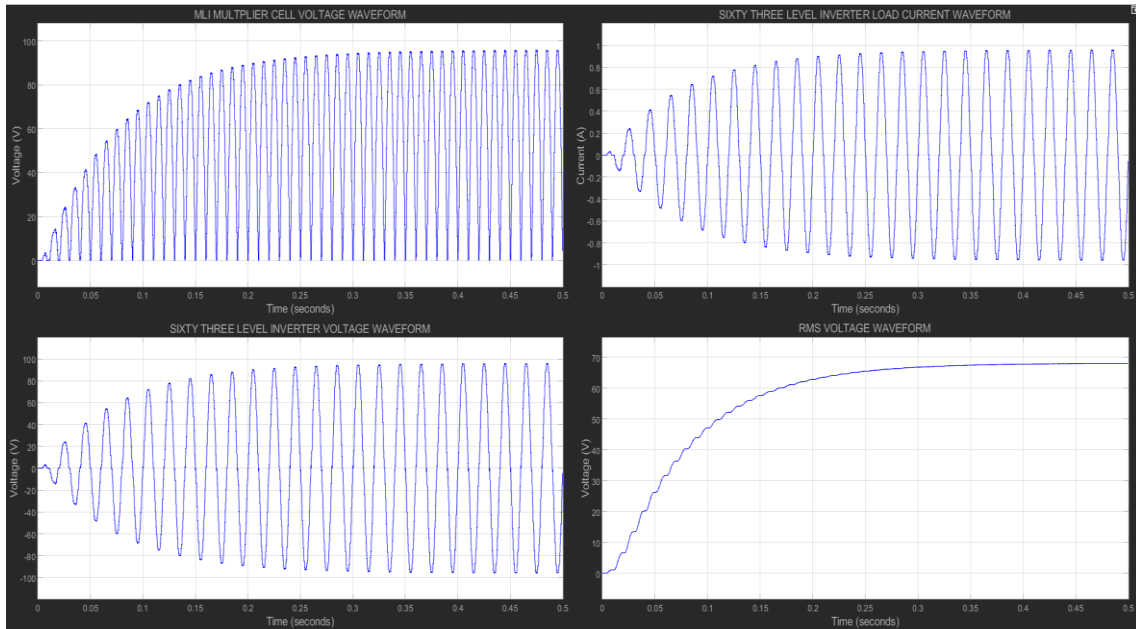


Figure 7: Simulation Result Waveforms

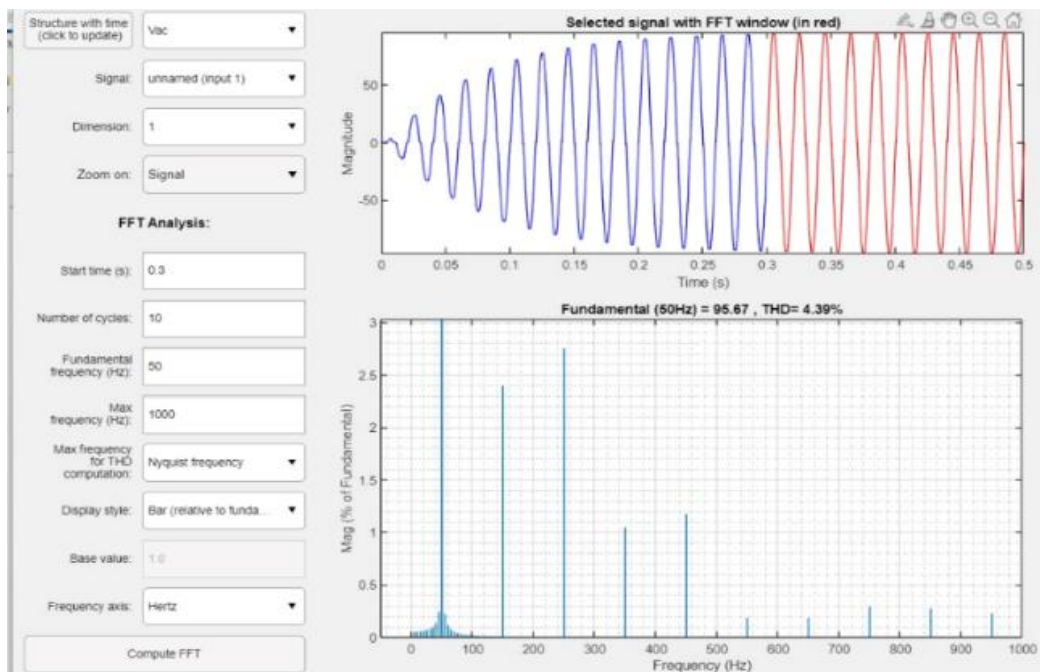


Figure 8: THD Output Result

The simulation shows the output results of a signal. The graph shows the magnitude of the signal in the frequency domain. The red line shows the magnitude of the signal with an FFT window applied. The FFT window is used to reduce the spectral leakage of the signal. The blue



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line shows the magnitude of the signal with no FFT window applied. The graph shows that the signal has a fundamental frequency of 60 Hz. The signal also has some harmonics, which are at frequencies that are multiples of the fundamental frequency. The THD (total harmonic distortion) of the signal is 4.39%. This means that the harmonics account for 4.39% of the total power of the signal. The number of cycles in the signal is 10. This means that the signal is 10 seconds long. The maximum frequency of the signal is 1000 Hz. This means that the signal contains frequencies up to 1000 Hz. The maximum frequency for THD computation is 500 Hz. This means that the THD of the signal is computed using the harmonics that are up to 500 Hz. The Nyquist frequency of the signal is 1000 Hz. This means that the signal is sampled at a rate of at least 2000 Hz. The graph shows that the magnitude of the fundamental frequency is the highest. This means that the fundamental frequency is the dominant component of the signal. The magnitude of the harmonics decreases with frequency. This means that the higher harmonics have less power than the lower harmonics. Overall, the simulation output results show that the signal is a 60 Hz sinusoidal signal with a THD of 4.39%.

Table 1: Comparison between R and RL load for a 63-level multilevel inverter

Parameter	R-Load	RL-Load
Load Type	Purely Resistive	Resistive-Inductive
Power Factor	Unity (1.0)	Lagging ($0.8 < PF < 1$)
Voltage Stability	Relatively stable	experience voltage fluctuations
Power Consumption	Active power only	Active and Reactive power
Real Power (W)	Consumes only real power	Consumes real and reactive power
Apparent Power (VA)	Same as Real Power	Higher than Real Power
Harmonic Distortion	Minimal harmonics	Have harmonic distortion d
Power Factor Correction	Not applicable	May require power factor correction devices
Efficiency	Typically higher	Slightly lower
Voltage Drop	Minimal	Voltage drop due to inductive component

6 Conclusion

A New 63 level inverter incorporated hybrid renewable energy source system for the generation of electric power is discussed in this Project [17]. The algorithms track the variation of voltage at dc-link and change switching frequency of flyback converter. To improve the gain of the system with minimum PV array and switching devices, a multiple stages of converters is utilized. The PI controller is adopted to attain a closed loop control and paves the way to obtain stable voltage [18].



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