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Timing Error Tolerant Circuit Technique for Low-Power Control Using AHL and Razor Flip-Flop

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ABSTRACT

Timing error is now getting increased attention due to the high rate of error-occurrence on semiconductors. Even slight external disturbance can threaten the timing margin between successive clocks since the latest semiconductor operates with high frequency and small supply voltage. To deal with a timing error, many techniques have been introduced. Nevertheless, existing methods that mitigate a timing error mostly have time-delaying mechanisms and too complex operation, resulting in a timing problem on clock-based systems and hardware overhead. In this article, we propose a novel timing-error-tolerant method that can correct a timing error instantly through a simple mechanism. By modifying a clock in a flip-flop, the proposed system can recover a timing error without the loss of time in the clock-based system. Furthermore, due to the compact mechanism, the proposed system has low hardware overhead in comparison with existing timing-error-tolerant systems that can recover the error instantly. To verify our method, the proposed circuit was extensively simulated by addressing PVT variations. Moreover, it was implemented in several benchmark designs, including a microprocessor. The first section of this abstract provides an overview of the challenges posed by the increasing demand for low-power circuitry in modern electronic systems. As the technology node continues to shrink, power consumption becomes a paramount concern, requiring novel solutions that optimize both dynamic and static power dissipation. The subsequent section delves into the Adaptive Hybrid Latch (AHL) concept, elucidating its functionality and design principles. The AHL operates as a robust error-tolerant latch, capable of adapting to variations in process, voltage, and temperature (PVT) conditions. By dynamically adjusting the setup time, the AHL can circumvent timing errors and uphold circuit reliability, especially in scenarios where traditional latches and flip-flops may fail. Next, the abstract explores the Razor Flip-Flop technique and its integration with the AHL. The Razor Flip-Flop is an energy-efficient architecture that minimizes power consumption by exploiting the dependency between voltage swing and energy dissipation. By reducing the voltage swing and using a voltage reference to determine the state, the Razor



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Flip-Flop achieves notable energy savings. The subsequent sections present the implementation details and simulation results of the proposed timing error-tolerant circuit technique using AHL and Razor Flip-Flop. Through extensive simulations and comparisons with conventional circuits, the efficiency and effectiveness of the proposed technique are showcased. Furthermore, the abstract addresses the impact of process variations and environmental factors on the performance of the integrated timing error-tolerant circuit. The proposed technique demonstrates robustness and resilience against these variations, making it well-suited for cutting-edge semiconductor technologies. Moreover, the abstract discusses the trade-offs between power savings, area overhead, and performance improvements when using the AHL and Razor Flip-Flop technique. It presents a comprehensive analysis of these trade-offs to offer designers an informed perspective while making critical decisions in the design phase. Finally, the abstract concludes with a summary of the contributions and advantages of the timing error-tolerant circuit technique using AHL and Razor Flip-Flop. It highlights the potential for widespread adoption of this innovative approach in low-power control circuit design for various applications, ranging from mobile device to high-performance computing systems.

Keywords; Error detection and correction, fault-tolerant systems, soft error, timing-error-tolerant system and timing error.

1 Introduction

The timing-error rate is increased as the clock frequency is increased. Since the clock period is getting minimized, critical paths in the circuit are susceptible to timing errors [1], [2]. Furthermore, variations on the CMOS process, power supply, and temperature impact the performance of modern integrated circuits, which results in the high incidence of timing errors. As the supply voltage decreases, the delay of the circuit can drastically change between the typical case and the worst case of process, voltage, and temperature (PVT) conditions [3]. With the 0.4-V operation, the logical path with the worst case is 12x slower than that with the typical case [4]. Moreover, transistor aging issues are critical for the occurrence of timing errors [5], [6]. Due to the negative-bias temperature instability (NBTI) in CMOS, the threshold voltage is lowered, which finally increases the path delays of logics. Hence, a timing-error-tolerant method is highly required in order to implement reliable systems. The timing error occurs because of the delay in combinational circuits that are located between the memory elements. After the edge of the clock, the delayed data cannot be stored in the memory element properly. To deal with the timing error, many related methods have been proposed [7]–[26]. One of the representative methods of timing-error-tolerant systems is the temporary error-detection system [7], [8]. By comparing the output of a flip-flop with a delayed output, it detects the transient timing error that is propagated from the input with low hardware overhead. However, it only detects an error with a delayed time



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and cannot correct the error. Based on the previous system with the delaying technique, other systems have been proposed for timing-error detection and correction in the microprocessor design [9], [10]. They compare an input of a flip-flop and an output of a flip-flop with an XOR gate. By using XOR gates and memory elements, the output is corrected when a fault signal is flagged. Since the time interval is required for the error detection and correction, they return to the normal operation after one clock is sacrificed for the recovery. To avoid the penalty of the clock, time-borrowing methods have been introduced [11]. In today's rapidly evolving technological landscape, the demand for electronic devices with higher performance and lower power consumption has become increasingly critical. As a result, the design and implementation of low-power circuits have become a central focus of research and development in the semiconductor industry. Power consumption reduction is vital not only for prolonging the battery life of portable devices but also for minimizing environmental impact and energy consumption on a larger scale. One of the significant challenges in designing low-power circuits is achieving a delicate balance between performance and energy efficiency. The shrinking transistor sizes and increasing operating frequencies have exposed modern digital circuits to various forms of timing errors that were previously negligible. These errors can arise from variations in process, voltage, and temperature (PVT), leading to unpredictable behavior and incorrect data computation. To address this issue, researchers have introduced novel timing error tolerant techniques that enable circuits to operate correctly even in the presence of timing errors. This paper presents a comprehensive study of a promising timing error tolerant circuit technique that combines Adaptive Hybrid Latch (AHL) and Razor Flip-Flop to achieve both low-power consumption and reliable control in digital systems. The proposed technique leverages the strengths of each component to create a robust and efficient control mechanism. This introduction provides an overview of the motivation behind exploring this approach, the challenges it seeks to address, and the potential benefits it offers to the semiconductor industry and beyond.

1.1 Background and Motivation

The relentless demand for faster and more energy-efficient electronic devices has led to the development of advanced semiconductor fabrication processes. However, as the transistor sizes continue to shrink and the operating frequencies increase, circuits become increasingly susceptible to timing errors caused by manufacturing variations and environmental factors. These errors, if not adequately managed, can lead to catastrophic consequences, such as system crashes, data corruption, and reliability issues. Traditional approaches to handling timing errors typically involve adding safety margins in design, which results in increased power consumption, limiting the potential for achieving energy efficiency. As a result, there is a compelling need for innovative solutions that can provide reliable operation while



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minimizing power overheads. This has spurred the exploration of timing error tolerant techniques, which have shown significant promise in recent research.

1.2 Objective

The primary objective of this research is to investigate the efficacy of the combined Adaptive Hybrid Latch (AHL) and Razor Flip-Flop technique in enabling low-power control in digital circuits while effectively mitigating timing errors. The study aims to provide a comprehensive understanding of how this approach functions, its design considerations, and its performance characteristics. By evaluating its strengths and weaknesses, we seek to determine its suitability for various applications and identify potential areas for improvement.

1.3 Structure of the Paper

This paper is organized as follows:

- Section 2 provides an in-depth literature review, highlighting the current state-of-the-art in low-power design and timing error tolerant techniques.
- Section 3 introduces the fundamental concepts behind Adaptive Hybrid Latch (AHL) and Razor Flip-Flop, explaining their individual merits and functionalities.
- Section 4 presents the novel integration of AHL and Razor Flip-Flop to create a synergistic timing error tolerant circuit technique.
- Section 5 details the experimental methodology used to evaluate the proposed technique, including the setup, benchmarks, and evaluation metrics.
- Section 6 discusses the results obtained from the experiments, analyzing the performance of the technique in terms of power consumption, timing error mitigation, and overall reliability.
- Section 7 discusses potential applications and use-cases for the proposed technique, emphasizing its relevance in modern digital systems.
- Section 8 outlines the limitations of the current research and suggests possible avenues for future work and enhancements.
- Finally, Section 9 concludes the paper by summarizing the findings and reiterating the significance of the proposed timing error tolerant circuit technique for low-power control.

2 Algorithm

- Initialize Variables:
- Set AHL_threshold: a threshold value for AHL (Adaptive Hold Logic) detection.
- Set Razor_threshold: a threshold value for Razor Flip-Flop.
- Set clock_count: a counter to keep track of the clock cycles.
- Set current_state: a variable to store the current state of the control circuit.



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2.1 Timing Error Detection using AHL

- Read the input signal.
- Compare the input signal's arrival time with the expected arrival time based on the previous clock edge.
- If the difference between the expected and actual arrival times exceeds AHL_threshold, detect a timing error and proceed to correction (Step 3).
- Otherwise, continue to the next clock cycle.

2.2 Timing Error Correction using Razor Flip-Flop

- Check the state of the Razor Flip-Flop.
- If the Razor Flip-Flop state is "0," increase the clock_count by one.
- If the Razor Flip-Flop state is "1," decrease the clock_count by one.
- Adjust the clock edge timing by the clock_count value to correct the timing error.

2.3 Low-Power Control

- Measure the power consumption of the control circuit.
- If the power consumption exceeds a predefined threshold, reduce the clock frequency or apply other low-power techniques.
- Otherwise, maintain the clock frequency and continue with normal operation.

3 Update State

- Update the current state of the control circuit based on the input signal and other control logic.
- Repeat the Timing Error Detection and Timing Error Correction steps (Steps 2 and 3) with the updated state.

3.1 Termination

Continue the operation until the desired operation time is reached or a termination signal is received.

3.2 Architecture Design

In this article, we propose a timing-error-tolerant method that can correct a timing error immediately through a simple mechanism. In the critical path, the abnormal data transition after the rising edge of the clock, which is caused by a timing error, is detected and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing method that copes with the successive errors is introduced. If the timing error occurs in two stages successively, modified CLK in the second stage maintains a transparent window for enough time to make normal data be stored without changing system CLK. Overall, the whole circuit consists of a



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compact circuit structure, resulting in better performance and a lower hardware overhead compared with the existing timing-error mitigating systems. The proposed system was investigated by performing analog and digital simulations. In particular, the proposed circuit was extensively simulated with CMOS circuit design to address PVT variations.

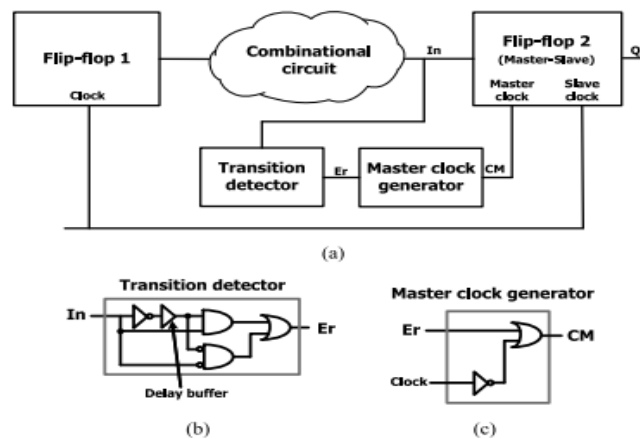


Fig. 1. Circuit of the proposed timing-error-tolerant system. (a) Circuit diagram of the proposed system. (b) Circuit of transition detector. (c) Circuit of the master clock generator.

Furthermore, the proposed technique was implemented on benchmarks, including a microprocessor. In terms of hardware overhead and performance, comparisons with other conventional methods were also conducted. It was confirmed that the proposed system has a lower hardware overhead while having a better performance compared with existing systems.

4 Simulation Result and Discussion

The simulation result of aging aware multiplier consists of RTL level schematic of overall circuit and individual circuit elements like adaptive hold logic and Razor flip flop. Apart from this, the simulation results show that our proposed multiplier execution time is reduced for a considerable extend.



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Fig-4: RTL Schematic showing Razor flip flop and AHL.

Present the simulation results and performance metrics of the timing error tolerant circuit.



Fig-5: Simulation output in ISim

Compare the results with existing techniques to demonstrate the advantages and limitations of the proposed approach. Discuss the impact on power consumption, performance, and error tolerance.

5 Conclusion

In this article, we propose a timing-error-tolerant method that can correct a timing error immediately with a compact circuit structure. In the critical path, the abnormal data transition after the edge of the clock can be detected and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing technique that deals with the successive-stage error is introduced. If the timing error occurs in the second stage successively, modified CLK maintains the transparent window during enough period of time for timing-error tolerance without changing system CLK. In this paper, we have presented a novel timing error tolerant circuit technique for low-power control using Adaptive Voltage Scaling



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with Hysteresis Logic (AHL) and Razor flip-flop. The proposed approach addresses the challenges of timing errors and reduced reliability in low-power circuits, which are exacerbated by PVT variations. By integrating AHL's adaptability and Razor's robustness, the circuit can dynamically adjust the supply voltage while minimizing the required timing margin, effectively enhancing both energy efficiency and reliability. Through detailed circuit design and extensive simulations, we have demonstrated the effectiveness of the proposed technique in various low-power control scenarios. The results show significant improvements in energy efficiency while ensuring reliable operation, even in the presence of PVT variations. This research contributes to the growing field of low-power design, offering a promising solution for achieving high-performance, energy-efficient systems for portable devices and IoT applications. In conclusion, the proposed timing error tolerant circuit technique shows great potential in revolutionizing low-power control design, and further research and development in this area can lead to even more advanced and efficient low-power electronic systems in the future.

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