



Article Title: High Speed Built in Self-Test via Pattern Generation

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ABSTRACT

This paper presents the built-in self-test (BIST) design of a C-testable high-speed carry-free divider which can be fully tested by 72 test patterns irrespective of the divider size. Using a graph labelling scheme, the test patterns, expected outputs, and control signals can be represented by sets of labels and generated by a simple circuitry. As a result, test patterns can be easily generated inside chips, responses to test patterns need not to be stored, and use of expensive test equipment is not necessary. Results show that the hardware cost for generating such labels is virtually constant irrespective of the circuit size.

Dividing Circuits, Integrated Circuit Testing, Integrated Circuit Design, Design For Testability, Digital Arithmetic, Built In Self-Test, Graph Theory, Built In Self-Test Design, High Speed Carry Free Dividers, C Testable Circuits, Graph Labelling, Test Patterns, Control Signals, 64 Bit, Built In Self-Test, Circuit Testing, Automatic Testing, Test Pattern Generators, Hardware, Signal Generators, Test Equipment, Costs, Controllability, Observability, In Spartan3E FPGA device family, computation of 8-bit circular convolution using Modified Karatsuba Algorithm

Keywords: DRAM fields, BIST, VLSI, polynomial Testability, Fault, LT-GLFSR.

1 Introduction

THE aggressive scaling of microelectronic technology is enabling the fabrication of increasingly complex ICs. Together with several benefits (improved performance, decreased cost per function, etc.), this poses serious challenges in terms of test and reliability [1] – [7]. In particular, during at-speed test of high-performance microprocessors, the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced BIST technology can also solve the problem that many circuits cannot be directly tested because they do not have direct external pins, such as embedded flash. It is foreseeable that even the most advanced ATE cannot fully test the fastest circuit in the near future, which is one of the reasons for using BIST.

2 Related Work

The Chinese name of BIST technology is built-in self-test technology, which can be applied to almost all circuits, so it is widely used in the semiconductor industry. For example, the BIST technology commonly used in DRAM includes implanting a test pattern generation circuit, a



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sequential circuit, a mode selection circuit, and a debug test circuit in the circuit. Intra-system digital data transmission techniques over backplanes and other transmission mediums have migrated from the use of relatively wide data busses with many data lines to the use of high-speed serial links with relatively few data lines. The serial approach can provide the same or greater aggregate bandwidth while simplifying the backplane design by eliminating a great deal of routing congestion and the need for trace length matching.

3 Architectural Design

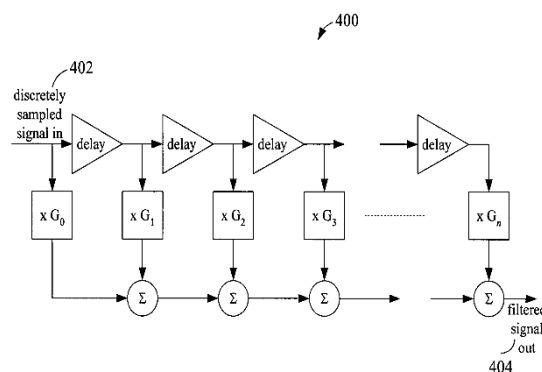


Figure 1: BIST for hardware implementation of (a)

This study presents a novel test pattern generation technique called Low-Transition Generalized Linear Feedback Shift Register (LT-GLFSR) with bipartite (half fixed) and bit insertion (either 0 or 1) techniques. Intermediate patterns (by bipartite and bit (either 0 or 1) insertion technique) inserted in between consecutive test patterns generated by GLFSR which is enabled by a non-overlapping clock scheme. This process is performed by finite state machine generate sequence of control signals. Low-Transition Generalized Linear Feedback Shift Registers (LT-GLFSR), are used in a circuit under test to reduce the average and peak power during transitions.

4 Background

The observed results demonstrate that when the identical characteristic polynomials are used in both the PRTPG and MISR-SAZ, then any change in initial loading of PRTPG does not change the value of aliasing count. Usually done at the logic level. Test patterns are then generated based on a defined fault model and applied to the manufactured circuitry. It has been proven mathematically that the generation of test patterns is an NP complete problem [27] and therefore different heuristics are usually used. Most of the existing hardware testing techniques work at the abstraction levels where information about the final implementation architecture is already available. Due to the growth of systems complexity these established low-level methods are not any more sufficient and more work has to be done at abstraction levels higher



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than the classical gate and register-transfer level (RT-level) in order to ensure that the final design is testable and the time-to-market schedule is followed.

4.1 Speed Way of Self-Testing

System-level synthesis: The specification of a system at the highest level of abstraction is usually given by its functionality and a set of implementation constraints. The main task at this step is to decompose the system into several subsystems (communicating processes) and to provide a behavioural description for each of them, to be used as an input for behavioral synthesis.

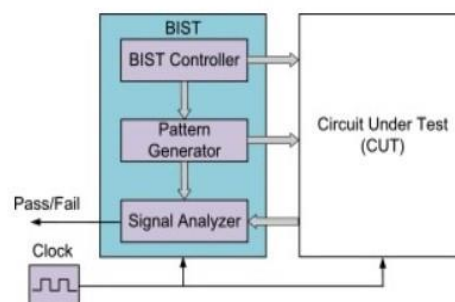
The output of the behavioural synthesis process

$$\begin{bmatrix} q_n(t+1) \\ q_{n-1}(t+1) \\ q_{n-2}(t+1) \\ \vdots \\ q(t+1) \\ q(t+1) \end{bmatrix} = \begin{bmatrix} c_n & c_{n-1} & \dots & c_2 & c_1 \\ 1 & 0 & \dots & 0 & 0 \\ 0 & 1 & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & 0 & 1 \\ 0 & 0 & \dots & 1 & 0 \end{bmatrix} \begin{bmatrix} q_n(t) \\ q_{n-1}(t) \\ q_{n-2}(t) \\ \vdots \\ q(t) \\ q(t) \end{bmatrix} \quad (1)$$

$$\text{where, } c_j = 0 \text{ or } 1, \text{ for } 1 \leq j \leq n-1 \text{ and } c_j = 1, \text{ for } j = n. \quad (2)$$

4.2 Modified Self-Test Pattern

In this section our Modified: Simulation results prove that this technique has reduction in power consumption and high fault coverage with minimum number of test patterns. The results also show that it reduces the peak and average power consumption during test for ISCAS'89 benchmark circuits.



4.3 Self-Test Pattern

The two most common categories of BIST are the Logic BIST (LBIST) and the Memory BIST (MBIST). LBIST, which is designed for testing random logic, typically employs a pseudorandom pattern generator to generate input patterns that are applied to the device's



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internal scan chain, and a multiple input signature register (MISR) for obtaining the response of the device to these input test patterns

5 Conclusion

In this paper, modified BIST enabled standard RAM is designed using VHDL and implemented successfully in Spartan 6 FPGA board. Every block of the proposed design is separately simulated and verified through Spartan6FPGA board before integrating into a single entity. Every simulated result and result from the FPGA board has exact parity. Multiplexers are used to maintain the same speed as of memory without BIST architecture when operating in the normal mode.

The device utilization and combinational path delay of MKM have been compared with standard 8×8 KM. It has been observed that the proposed multiplier has better timing performance than standard KM. In Spartan3E FPGA device, proposed multiplier needs 14.9% lesser delay than KM, and it also consumes 45.5% lesser slices compared to KM. The new architecture is very simple and easy. This feature is advantageous to have a suitable trade-offs between area and speed for implementing circular convolution algorithm in VLSI. In FPGA device family, computation of 8-bit circular convolution using MKA is 26.5% faster than KA. It also consumes 61.7% less slices than existing KA based convolution. MKM may also be used to design cryptosystems. Proposed multiplier is faster and hardware efficient compared to existing Karatsuba multiplier.



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