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Efficient Low-Power Timing-Error Control in Digital Integrated Circuits Using Timing Error-Tolerant Circuits and Time-Borrowing Techniques

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ABSTRACT

In modern digital systems, real-time operation of integrated circuits is of paramount importance. Presently, a significant portion of energy consumption is attributed to the overhead incurred by accommodating worst-case scenarios. This research proposes an energy-efficient timing-error control method employing a circuit designed to tolerate timing errors. The critical path is adept at identifying and correcting timing errors, particularly those causing irregular data transitions following the rising edge of the clock. Management of the transparent window of the clock is instrumental in swiftly addressing timing faults using minimal logic. A novel time-borrowing technique is introduced to account for future errors, applicable to locations with a short flip-flop setup time. The timing mistake occurs in two stages, and during second stage, an organized clock ensures a sufficiently extended transparent window, allowing for preservation of regular data without necessitating alterations to system clock. The study utilizes Razor Flip-flop and Adaptive Hold Logic to detect and recover from timing issues. This low-power timing-error control method provides an efficient means of mitigating the energy overhead associated with worst-case scenario margins in real-time digital systems.

Keywords: Adaptive Hold Logic (AHL), Flip Flop (FF), Combinational Logic Circuits, Transition Detector, RAZOR FLIP-FLOP.

1 Introduction

Electrical circuits are classified into two categories: combinational circuits and sequential circuits. In this work, combinational circuits are used. A well-equipped system will only increase the requirement for electronic equipment. Careful electronic circuit design is therefore necessary. Subtle design changes cause serious circuit problems [1]. Errors occurs by a variety

of variables, including changes in temperature, pressure, vibrations, and the wrong component selection for the circuit. Timing problems are one important kind of error that happen in circuits. Combinational circuit timing issues result from a variety of factors. Delays may impair the complete operation of electrical devices [2]. It resulted in a decline in client demand for that particular device. A suitable technique for repairing such a timing fault circuit should exist. But owing to certain restrictions, an alternative approach is employed. There are numerous methods available to solve this issue [3]. In some ways, the obstacles that prevented them from reaching the objective. Therefore, to recover the timing error circuit, Adaptive Hold Logic (AHL) is used, not just to identify errors but also to fix them. Numerous methods were employed to identify or prevent timing errors [4]. Some of the current systems use time borrowing, which reduces timing inaccuracy in a circuit by borrowing a portion of the current clock cycle from later stages. However, the implemented circuit proved difficult to implement due to its complexity. A regulating clock is used to detect the timing fault tolerant circuit in another way [5]. This method was carried out by utilizing the clock's transparency. The output flip-flop's clock will become active and receive input at the appropriate time if the input arrived on time. The clock becomes non-transparent for the output flip-flop for a while to allow the current clock to finish the operation if the input exits the combinational circuit after a little delay [6]. Then, just the second flip-flop received input and turned on after receiving a clock. It is putting up with the timing error in this way. However, this is merely a method for finding the mistake. Therefore, in order for this work to perform properly, another logic must be adopted [7]. The reasoning is known as "adaptive hold logic." The timing error circuit is recovered by employing the AHL circuit. Holding the clock pulse for a predetermined period of time is what to do when a timing infraction interferes with a subsequent stage's ability to operate [8]. A straightforward counter in the AHL circuit displays if there has been a noticeable decline in the circuit's performance. The counter keeps track of the transition detector's errors over a predetermined amount of time [9]. The circuit has experienced severe timing deterioration as a result of the combinational logic if the timing violations are greater than a predetermined threshold. After that, AHL will output 0 to turn off the flip-flops' clock signal. In the event if not, the AHL will output 1 for regular operations [10]. The system's efficiency is increased by using a timing error-tolerant circuit and the time borrowing approach to remove successive-stage errors. Transition detector: a tool to prevent errors in data transmission. The list below demonstrates how the paper is organised: Section I gives a description of the introduction. The recent works are described in Section II. The proposed model and description are explained in Part III. The results are presented in Section IV. In Section V, the conclusion is presented.

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2 Recent Works

Mehrnaz Ahmadi *et al* [2019] [11] have developed a method for avoiding dynamic timing errors in high-performance architectures that uses predictive logic. The critical feedback path and successive critical path structures' timing violations, however, cannot be avoided by it. A revolutionary concept that combines dynamic clock stretching in SCP and CFP structures with output of the critical path's fast prediction logic. In addition, there is more performance enhancement using this strategy. Timing violations in problematic path structures cannot be prevented using the DFFC approach.

Thierry Bonnoit *et al* [2018] [12] have described VLSI circuits increase fault tolerance by lowering the rollback cost. Circuits are becoming increasingly susceptible to several types of disturbances in nanoscale technologies. Single-event disturbances caused by alpha particles and atmospheric neutrons impact flip-flops, latches, and memory cells. There are already techniques for identifying errors in logic functions, but the number of alternatives that provide repair is limited, resulting in significant hardware overhead in non-processor architecture. This innovative method lowers the cost of rollback in all types of circuits by combining many hardware architectures with an algorithm for their implementation.

Zhen Gao *et al* [2018] [13] have presented unique most widely utilized procedures in current digital signal processing and digital communication systems is matrix-vector multiplication, or MVM. In many systems, parallel matrix processing is a common practice. This work suggests an integer parallel MVM design that is fault resilient. Error repair code concepts are combined with MVM's self-checking feature in this system. It follows that in real-world applications, the proposed method can help lower the expense of providing fault tolerance. The proposed approach is not extended in this study to address numerous faults.

Guangda Zhang *et al* [2018] [14] have examined a physical-layer impasse is caused by repeated failures in quasi-delay-insensitive networks-on-chip. In large-scale many-core systems, networks-on-chip (NoCs) provide efficient and scalable on-chip communication fabrics. To protect the NoC data paths that comprise approximately ~ 90% of the logic, the suggested detection technique has been implemented. The network function is recovered with a slow fall in performance, and a permanently damaged connection is precisely detected by applying the interrouter link detection and recovery methods (~ 60% of the logic). Support for adaptive routing provided by the routing layer is typically needed for recovery from router data-path problems; this is left for future study.

Yan Li *et al* [2017] [15] have presented soft-error tolerance, a brand-new complementary dual-modular redundancy, or CDMR, approach is put forth. But the big area overhead and the voter's vulnerability are two serious flaws in the original TMR. A two-stage voting system, consisting of a second-stage high-performance merging unit and a first-stage optimized MRF structure, is constructed in complementary dual-modular redundancy, with inspiration from Markov

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random field (MRF) theory. To address these shortcomings, a novel complementary dual-modular redundancy (CDMR) technique was proposed to mitigate the impact of soft mistakes. Out of all the designs, the recommended method continues to have the lowest output error rate.

3 Proposed Work Explanation

This research uses adaptive hold logic to propose a recovering timing error circuit. When FF1 sends input data to the combinational circuit. In the event that the combinational circuit's output is delayed, the transition detector produces an error signal. It is handed off to AHL logic. The counter and comparator make up the majority of AHL logic. The AHL logic counter will be used to count the errors that occur during transitions. If the comparator's threshold value is exceeded by the counter value. The gating signal is one when the counter value is less than the threshold value. Every time counter rate rises above threshold rate, the gating signal will turn zero. The circuit block for time borrowing is used to modify the delayed time. Another block dubbed a razor flip-flop is used in the proposed work. The error signal counts whenever the transition detector notices a change in the combination circuit's output. However, it doesn't say whether the transition is happening at the right time or the wrong time. To determine if a transition is occurring at the right or wrong time, utilize a razor flip-flop. The Adaptive Hold Logic recovers timing errors. Timing faults are identified and recovered from with the use of the mentioned Razor Flip-flop and Adaptive Hold Logic.

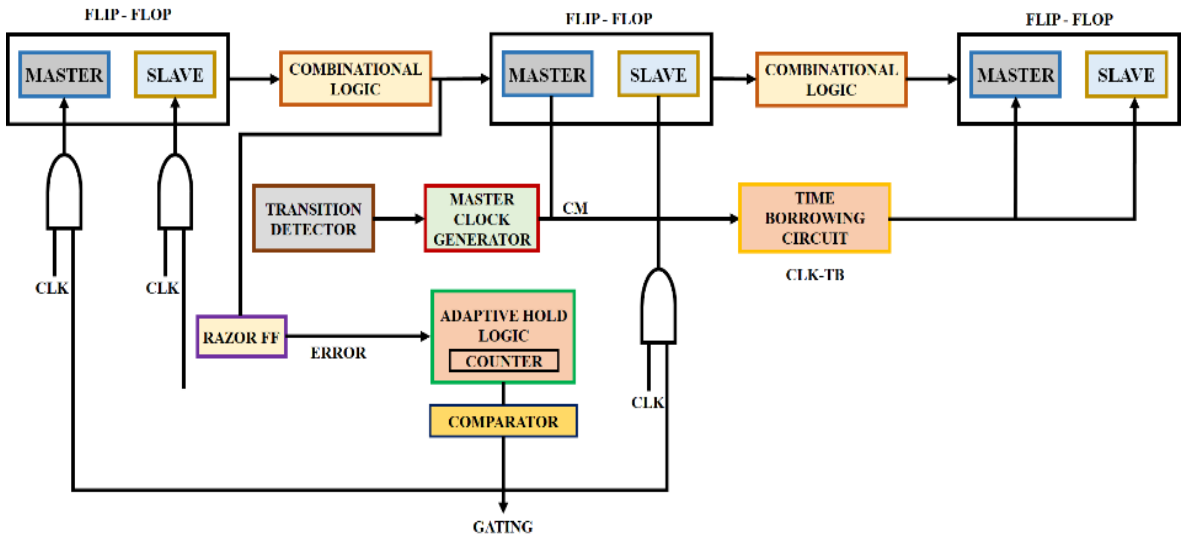

Figure 1: *Block diagram for proposed system*

3.1 Flip Flop

A Flip Flop is a single bit information that can be stored in a memory element. Because it has two stable states—0 and 1—it is often referred to as a bistable multivibrator. A flip-flop is a

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binary bit storage device that has two states: "0" is represented by one state, and "1" by the other. Sequential logic is the term for the comparable circuit used in this sort of data storage, which is utilized to store states. In electronics, bistable multivibrators, or flip-flops and latches, are two stable state circuits that are capable of storing state data. A circuit may change state in response to signals applied to one or more control inputs; once changed, the circuit will output that state (and occasionally its logical complement as well).

3.2 Master Slave Flip Flop

JK flip flops are connected in series, one serving as the slave and other as the master, is used to create a master-slave flip flop. The master flip flop's output is connected to both of the slave inputs. Furthermore, the slave flip flop's output receives the inputs from the master flip flop. A device or process (referred to as the "master") serves as the communication hub and controller of one or more other devices or processes in the master/slave model of asymmetric communication or control.(referred to as "slaves").

3.3 Master Slave FF Working

The slave once detached the CLK pulse swings too high, which indicates 1; however, inputs like J and K may alter the system's state. The slave is capable of separating from FF until the CLK pulse becomes low, or zero. Whenever the CLK pulse returns to low-state, data is transferred from the master FF to the slave FF, allowing the o/p to be obtained. Slave Flip Flop will first be triggered at a negative level while the master FF will initially be triggered at a positive level.

3.4 Combinationational Logic Circuits

Circuits with a variety of logic gate types are known as combinational logic circuits. Simply put, a circuit that combines different kinds of logic gates is known as a combinational logic circuit. The output of a combinational circuit is determined by the current combination of inputs, regardless of the previous input. Input variables are the fundamental elements of a combinational logic circuit, output variables, and logic gates. Adder, subtractor, divider, encoder, multiplexer, and de-multiplexer are examples of circuits using combinational logic. Because NAND and NOR gates are thought of as "universal" gates, any combinational circuit is constructed using just these two gates.

3.5 Transition Detector

A transition detector is utilized in flip flop circuits to accomplish edge triggering. It merely creates an extremely narrow pulse from the clock signal's rising edge. It is made up of the clock signal itself, which is inverted after going via a NAND gate, and a delay gate. The benefit of edge triggering is that it does away with the issues that pulse-triggered flipflops (like master-slave flip flops) have with zero and one catching.

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3.6 Master Clock Generator

The device that transmits the clock signal to the synchronization device or devices is called a Master Clock Generator. Digital devices that have clock input terminals installed receive external clocks from the master clock generator, an incredibly reliable oscillator. As a member of the clock network, the linked devices are known as "slaves," and they are synchronized with the master clock. It converts and distributes one or more accurate timing reference signals to other devices in order to increase the precision of those timing references. Applications and sectors that use master clock systems include aerospace and defence.

3.7 Time Borrowing Circuit

A longer path borrow time by using a technique called time borrowing from the subsequent logic's next path. Time borrowing usually affects the setup by slowing down the delivery of data, which leads to a prolonged arrival time. The time of the following path follows a deduction from the time the latch borrowed from the next section of the pipeline.

3.8 Adaptive Hold Logic (AHL)

This variable-latency multiplier circuit's main component is the Adaptive Hold Logic circuit. A D flip-flop, MUX, and decision block are components of the AHL circuit. Timing violations result from the column-bypassing multiplier's inability to carry out these operations properly if the cycle duration is too short. The Razor flip-flops, which produce error signals, will detect these timing problems. If errors occur regularly, the aging effect has caused severe timing degradation in the circuit. Upon receiving an input pattern, the decision block determines if it needs to be completed in one cycle or two and sends the results to the multiplexer. It is the essential part of the variable latency multiplier that is age-aware.

3.9 Razor Flip-Flop

The Razor flip-flops detect if there is a timing violation or path delay. A shadow latch, multiplexer, XOR gate, and primary flip-flop are all components of a 1-bit Razor flip-flop. Timing violations indicate that the multiplier's execution result is wrong and that the cycle period is insufficient for the present operation to finish. In order to confirm that this current operation is proper, the Razor flip-flops will thus output an error to alert the system that a second cycle of the operation is required.

4 Results and Discussion

The Xilinx ISE Design Suite 13.4 software is used to analyze the simulation findings. With the help of a full array of software tools, setup wizards, IP, and integrated development environments, the ISE Design array System Edition makes design easier and makes full use of the flexibility that comes with programmable platforms. With ISE, a developer synthesize (or

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"compile") their designs, analyze timing, study RTL diagrams, test how a design responds to various stimuli, and set up the target device in conjunction with a programmer. The Embedded Development Kit (EDK), Software Development Kit (SDK), and Chip Scope Pro are additional parts that come with the Xilinx ISE. While ISIM, or the Model Sim logic simulator, is utilized for system-level testing, the Xilinx ISE is primarily used for circuit synthesis and design.

The Reed-Solomon block is joined with the Mag Check block. In order to determine the packet type, a PID check is started using the control signal En_PID if the arriving data point is 8'b1000_0000 (SYNC field). Upon En_PID being 0, the Mag check block ceases to function. Stated differently, the SIE module enters a condition of suspension anytime it receives data that is consistently high. The received data remain unaltered and the valid data control line drops to zero in the suspended condition. When the reset signal gets high (1) and the full flag shows, the SIE module restarts and continues with the data processing stages. The SIE module runs in the idle state without obtaining the subsequent input data point as long as the transmitted data are valid. The PID check block ascertains whether the serial data conforms to the USB packet format following the parallel input data's conversion into serial data by the Reed-Solomon block. The CRC5 check is performed if the serial data are certificate packets (tokens); if not, the information packet's (data) CRC16 checksum is shown. Thus, data are conveyed through the bit-stuffing blocks and symmetric encoder after passing through the multiplexer. The serial data are transmitted to the recipient's end after the previously described tests are finished.

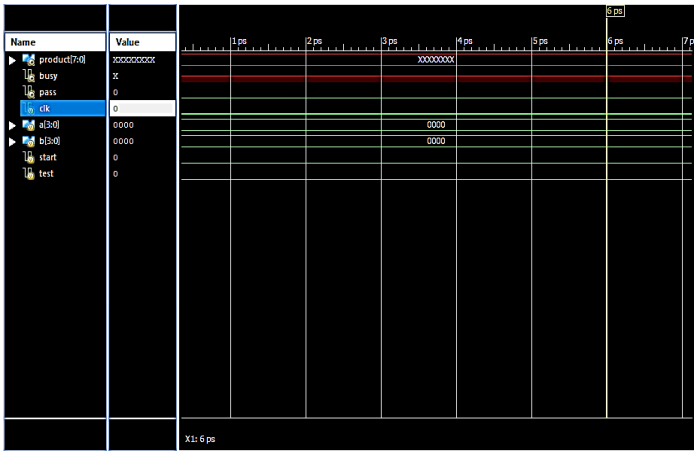

Figure 2: *Simulation Result*

The simulation results based on the supplied data are displayed in Figure 2. The red line indicates errors.

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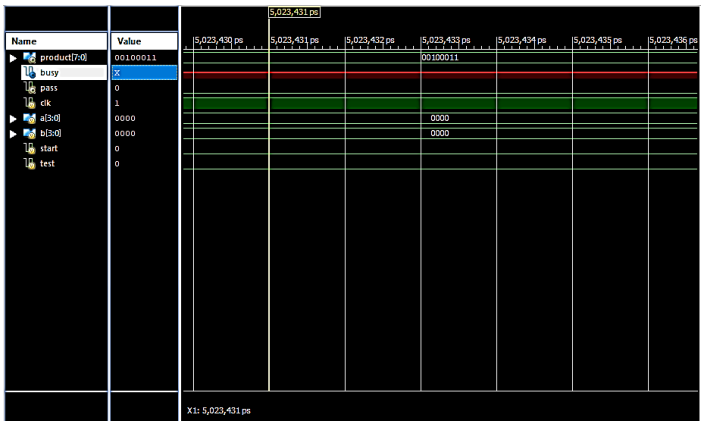

Figure 3: *Simulation Result*

Figure 3 illustrates how the simulation's mistakes decrease with changing input values.

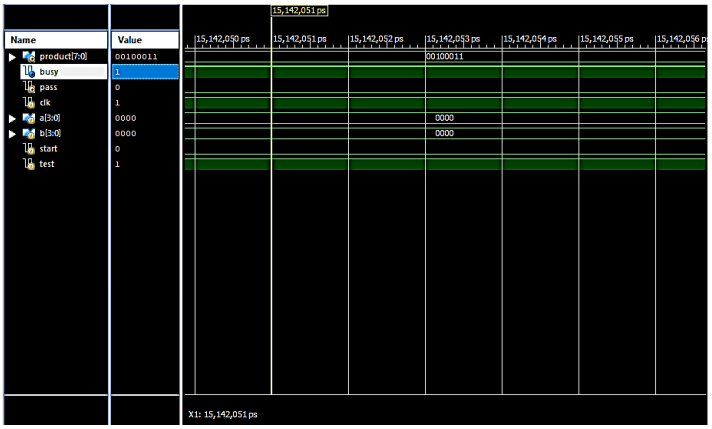

Figure 4: *Simulation Result*

The results of the simulation are aptly illustrated in Figure 4.

5 Conclusion

This work proposes a timing error-tolerant technique that uses a small circuit structure to quickly fix timing errors. A timing error-tolerant circuit is utilized to provide an efficient means of identifying and rectifying timing faults; the mechanism of the tolerant circuit involves time borrowing. The Razor flip-flop is utilized to determine whether the transition is occurring at the right or incorrect time, and Adaptive Hold Logic (AHL) recovers timing errors. The specified Razor Flip-flop and Adaptive Hold Logic will assist in identifying and resolving timing issues.

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