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Article Title: Implementation of Ripple Carry Adder Design for Optimal VLSI Performance

Implementation of Ripple Carry Adder Design for Optimal VLSI Performance

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ABSTRACT

In the province of wireless receivers, biomedical equipment, and portable/mobile devices, the demand for Very Large Scale Integration (VLSI) systems that optimize space, minimize power consumption, and deliver high performance is dominant. At the core of these systems, adders play a pivotal role as the primary component of arithmetic units. This paper proposes a ripple carry propagate adder with a high-speed area-efficient. The two's complement representation is employed for adding two numbers, a common practice in various systems dealing with n-bit input sequences. Microprocessors and digital signal processing use these carry adders. The carry output of every finished adder stage is useful as a carry input to the one behind it. This procedure is continued until the last complete adder stage is reached. Each carry output bit in an entire adder is therefore rippled to the next stage. An exact (forward) carry adder be linked with the proposed structure to generate hybrid adders with tunable accuracy levels. The practical implementation of proposed model is carried out using Xilinx ISE Design Suite 13.4, showcasing its feasibility for real-world applications.

Keywords: Ripple-Carry Adder (RCA), Digital Signal Processing (DSP), Full-Adder (FA), FIR Filter, Ripple Carry Adder Delay.

1 Introduction

The adoption of design techniques to enhance noise immunity in modern integrated circuits is an inherent cost in this new era of VLSI design. The challenge is compounded by synergy of little supply voltages and diminishing device sizes, contributing to increased variability across various features of the device. [1]. Variability in procedure is ascribed to the disparity in production tolerances as well as technological scaling, astounding advancements in physics that occurred in the 20th century have earned it the moniker "Quantum Century." [2]. A major factor in the caliber and scope of these innovations, especially in the later part of the 20th century, was the introduction of the digital computer a vital instrument with enabling them to take on challenges that had previously been thought to be insurmountable [3]. The digital

computer is currently the most useful instrument for physics research of all time, physicists be interested in the theory and design of computers and existed for thousands of years [4]. The Greek Antikythera and other ancient computers were complex, solely mechanical; later computers used large vacuum tubes to efficiently control the flow of electric signals; and most contemporary computers are made up of enormous arrays of transistors that execute billions of calculations per second [5]. Digital inputs and outputs, which operate with either high (on) or low (off) signals, are a common feature shared by the majority of these devices [6]. Specifically, transistors have shown to be essential for building digital circuits because they are extremely effective electronic switches. [7]. Primary objective of this work is to investigate the many arithmetic and logical operations carried out on electrical signals using transistors [8]. The building of a basic binary addition arithmetic logic unit will be the exclusive emphasis, despite the fact that transistors form the foundation of practically every component found in a modern computer, including memory, storage, and CPUs [9]. In order to comprehend the principles of electrical switching, the construction of field-effect and bipolar junction transistors, then go over an overview of Boolean algebra in order to investigate the mathematical foundation of arithmetic and logical operations and execute a 4-bit ripple-carry adder using this theoretical framework [10]. To decrease area, power, and delay by RCA, boost productivity and power efficiency by using a complete adder, and develop a ripple adder with a high degree of efficiency. The list below demonstrates how the paper is organised: Section I gives a description of the introduction. The recent works are described in Section II. The proposed model and description are explained in Part III. The results are presented in Section IV. In Section V, the conclusion is presented.

2 Recent Works

Sathyakala *et al* [2021] [1] have explained linearity and reliability of the FIR filter make it a crucial component of the digital world. Since multiplier and adder units are the fundamental components of FIR filters, lowering their number will increase the area efficiency of the filters. Within the VLSI architecture of the FIR filter, three operand binary adder algorithms are employed. A fundamental functional unit in modular arithmetic is the binary adder with three operands. Using recomputed bitwise addition and carry-prefix calculation logic, three-operand binary addition is accomplished. It reduces power, area, and latency significantly.

Harish Kumar *et al* [2022] [2] have described that in many cryptography and pseudorandom bit generator (PRBG) approaches, modular arithmetic is performed using the three-operand binary adder as the fundamental functional unit. Three-operand addition uses a square root carry choose adder, which results in a large reduction in critical path delay at the expense of additional hardware. A novel high-speed and area-efficient adder architecture is proposed by RCA logics that completes the three-operand binary addition with a significant reduction in

area, low power, and adder latency. The design is implemented on an FPGA device and is created using a 32nm CMOS technology library that is sold commercially.

Nagarjuna *et al* [2021] [3] have explained the most important unit in every electronic device is the arithmetic and logic unit. As of late, an arithmetic and logic unit's significance has been attributed to its ability to perform efficient algorithmic operations, including addition and multiplication. In several encryption techniques and pseudorandom bit generator (PRBG) approaches for modular arithmetic, the fundamental functional unit is the three-operand binary adder. In order to do three-operand binary addition with significantly less area, low power consumption, and adder latency, a revolutionary and incredibly efficient adder architecture is proposed. This adder architecture uses pre-compute bitwise addition followed by carry prefix calculation logic.

Swathi *et al* [2021] [4] have described to identify potential areas for area reduction, the binary tree adder (BTA) based on (RCA) is examined. Analysis is used to determine the critical path of carry for the new logic implementation, and an appropriate RCA design for the BTA. With m bits (m=8, 16, and 32 bits), the RCA is designed to be more efficient than the present RCA in terms of area and time. The multi-operand adder (n=8, 16, 32) BTA structure is proposed using this RCA architecture. The combination is done using 22nm CMOS technology.

Sivakumar *et al* [2021] [5] have proposed the basic building blocks of many cryptography and pseudorandom bit generating (PRBG) systems are three-operand binary adders. The carry-save adder is the method most often used for adding three operands. A new high-speed and area-efficient adder architecture is created that can execute three-operand binary addition with significantly less area, low power consumption, and adder latency by using pre-compute bitwise addition followed by carry-prefix computation logic. Less area, less power dissipation, and a shorter delay are characteristics of the HC3A adder. Employing the adder, aim for low ADP and PDP.

3 Proposed Work Explanation

The primary goals in designing digital processing units are to minimize power consumption and boost speed, especially for portable devices. Making the sacrifice of computational precision is one technique to get more power and faster processing. When some degree of error is acceptable, approximate computation is one technique be used. Ripple-carry adders are commonly used in traditional binary arithmetic to add integers. They consist of Full-Adder (FA) cells connected in a sequential manner, with the carry-out output of the preceding FA driving the carry-in input of the subsequent FA.

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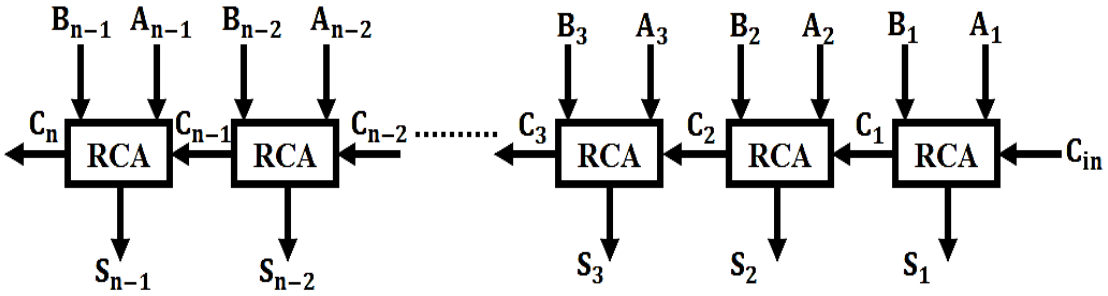

Figure 1: *Proposed Block diagram*

This proposed work provides an area-efficient, high-speed method by using ripple carry adders. An addict to 4 bits may change inputs 1111 and 0000 to 1111 and 0001 as their entry mode for case propagation. That's what happened—from 01111 to 10000. The easiest Adder to employ in VLSI digital design is this one. All that's needed to make an N-bit RCA is to design, sort, and sequence those N pieces. The FA band concert sets the overall pace for the RCA. The FA (t) RCA prompt will be reduced while going via the channel with a longer RCA bearing. To reduce the period it proceeds to process applications, FA group's application may be chosen.

3.1 Ripple Carry Adder

A half adder is used in digital electronics to add binary values with two bits. If the input sequence consists of a three-bit sequence, finishing the addition operation with a complete adder is also an option. However, if the input sequence has more bits than necessary, a half adder be used to finish the operation. Because the addition operation cannot be completed by the entire adder. Consequently, "Ripple Carry Adder" be used to get around these problems. For adding N-bit values in digital processes, this particular kind of logic circuit is employed. An introduction to ripple-carry-adder technology and its use is provided in this article. Until carry outputs from each complete adder stage are generated and passed to the next stage, the entire output of this carry adder remains unknown, which is one of the most crucial factors to take into account. As a result, using this carry adder will cause a delay in getting the results.

3.1.1 4-Bit Ripple-Carry Adder

The 4-bit ripple-carry adder is depicted in the diagram below. Four complete adders are cascaded together inside this adder. The carry input bit, Co, is always less than zero. The output is represented as S1 S2 S3 S4 and output carry C4 when this input carry 'Co' is applied to the two input sequences, A1 A2 A3 A4 and B1 B2 B3 B4.

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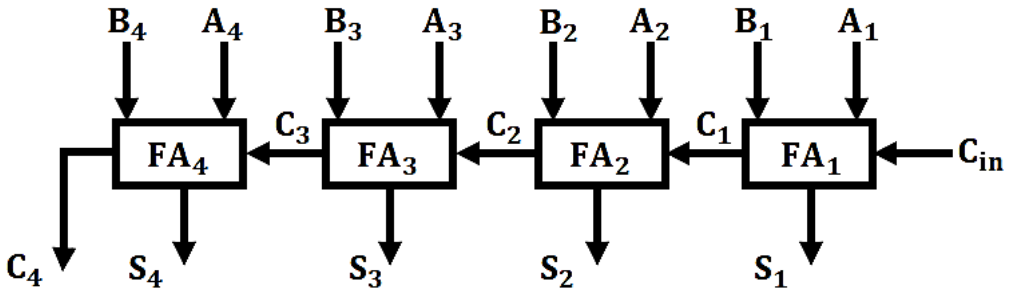

Figure 2: *4-Bit Ripple Carry Adder*

3.1.2 8-Bit Ripple Carry Adder

Eight complete adders connected in a cascading fashion make up this structure. Each full adder carry's input carry is coupled to the output of the subsequent stage full adder. While the input sequences are represented by (A1 A2 A3 A4 A5 A6 A7 A8) and (B1 B2 B3 B4 B5 B6 B7 B8), the proper output sequence is indicated by (S1 S2 S3 S4 S5 S6 S7 S8). A 4-bit ripple-carry-adder is used to add bits in an 8-bit RCA; that is, it adds the input carry and each bit from the two input sequences. This will be put to use when two 8-bit binary digits are added.

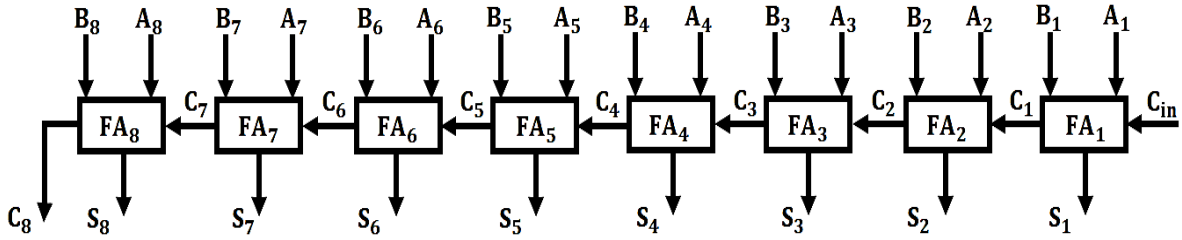

Figure 3: *8-Bit Ripple Carry Adder*

3.1.3 16-Bit Ripple Carry Adder

It is equipped with sixteen complete adders connected in a cascading fashion. Each full adder carry's input carry is coupled to the output of the subsequent stage full adder. While A1... A16 and B1..... B16 represent the input sequences, S1.... S16 denotes the pertinent output sequence. With input carry, every bit from two input sequences will add up in a 16-bit ripple-carry adder, which works similarly to a 4-bit ripple-carry adder. This will add two binary digits that are 16 bits long.

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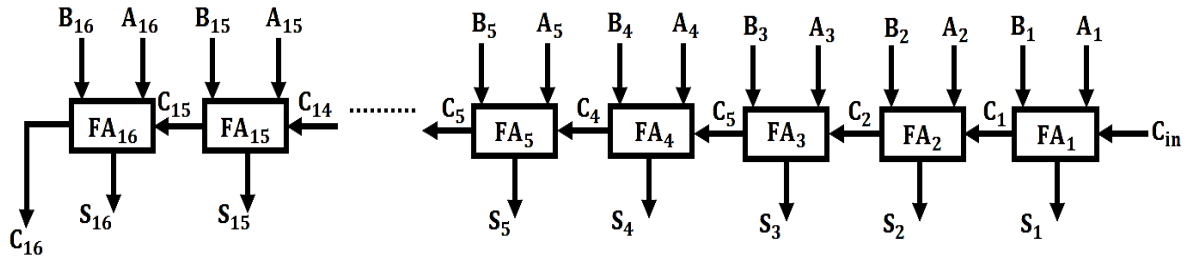

Figure 4: *16-Bit Ripple Carry Adder*

3.2 Ripple Carry Adder Delay

After generating the carry from the previous stage, the output of the ripple carry adder is known. The carry signal must therefore ripple through the adder from the least significant step to the most significant stage before the sum of the most significant bit is accessible. As such, before the final total and carry bits become valid, there will be a considerable wait. For simplicity's sake, Table 4.2 displays the delays for a number of CMOS gates assuming that each gate is loaded equally. Every delay is standardized in relation to the simple inverter's delay. Additionally, the relevant gate areas normalized to a basic minimum-area inverter are displayed in the graphic. Note that multiple-input gates necessitate a different circuit technique than simple circuits, as shown in the table.

Table 1: *Areas normalized in relation to an inverter and CMOS gate delays*

GATE	DELAY	AREA	COMMENT
Inverter	1	1	Minimum delay
2-input NOR	1	3	More area to produce delay equal to that of an inverter
2-input NAND	1	3	More area to produce delay equal to that of an inverter
2-input AND	2	4	Composed of NAND followed by inverter
2-input OR	2	4	Composed of NOR followed by inverter
2-input XOR	3	11	Built using inverters and NAND gates
η-input OR	2	$\frac{\eta}{3}+2$	Uses saturated load ($\eta > 2$)
η-input AND	3	$\frac{4\eta}{3}+2$	Uses η −input OR preceded by inverters ($\eta > 2$)

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Estimate the delays related to RCA stages' outputs, as shown in Table 2, using Table 1 and the 2 schematic. In relation to an inverter delay, the delays are normalized.

$$SumS_{\eta-1}delay = 4\eta + 2 \quad (1)$$

$$CarryC_{\eta}delay = 4\eta + 3 \quad (2)$$

The carry chain normalized delay for a 32-bit CPU be 131. When adding a large number of bits, the ripple carry adder may become extremely sluggish. Actually, the majority of microprocessor speeds are defined by the propagation delay of the carry chain.

Table 2: *Four-bit RCA output delays adjusted to an inverter delay*

Signal	Delay
S_0, C_1	6, 7
S_1, C_2	10, 11
S_1, C_3	14,15
S_3, C_4	18,19

3.3 FIR Filter

A filter is a device or system that removes an unwanted component or feature from a signal. Filtering is a kind of signal processing that denotes the whole or partial removal of specific signal components. Analog and digital filters are the two main types that are offered. Filters be categorized into numerous groups based on the criteria used for classification. Digital filters for Finite Pulse Response (FIR) and Digital Filtering (IIR) are the two primary types of optical filters. It is difficult to build a broad order FIR filter in real time in a resource-constrained environment since the FIR method does not include redundant computing. The filter coefficients often remain constant and have established signal processing applications.

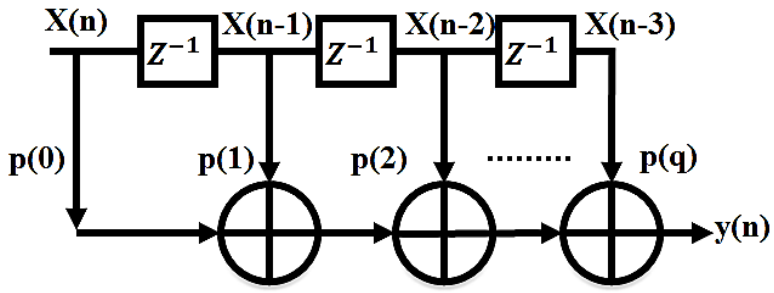

Figure 5: *Finite Impulse Response Filter*

$$out(n) = \sum_{i=0}^{N-1} x(n-i)h(i) \quad (3)$$

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Where the filter coefficients are denoted by {h (i): i = 0… N-1}. Convolution is carried out via a filter, which is often built with infinite signal durations in mind. On the other hand, boundary discontinuities are present in limited duration signals, such as images. The number of additional samples at the signal borders is equal to N-1. It's possible that the left and right signals are divided unevenly. Both α and μ be used to hint at the number of samples the input's left and right sides (α+μ=N-1).

4 Results and Discussion

The study examines the design parameters of both the hybrid adders that are implemented utilizing the RCPFAs and those that are not. The Synopsys HSPICE tool, which is based on 45-nm Nan Gate technology, is used to perform this work. For each simulation, the supply voltage was fixed at 1 V and the temperature was maintained at 25 °C. A simulation is performed for the energy (delay) of an inverter for the scenarios FO1 and FO4, yielding values of 0.64 fJ (22.7 ps) and 1.71 fJ (42.3 ps), separately, to get a sense of the technological characteristics. Initially, a comparison is made between the parameters of the exact FA and the RCPFAs. By using every possible combination of inputs, the power and energy have been retrieved. The RCPFA-II (RCPFA-III) has transistor counts that are, respectively, 55% (19%), 70% (56%), 38% (29%), 70% (60%), and 29% (29%), lower than those of the identical FA.
The supply voltage Vdd = 1.2 V and frequency of 100MHz were used for the simulations. A comparison with current or previously published designs is provided to highlight the advantages of the 1-bit adders and their good power delay product.

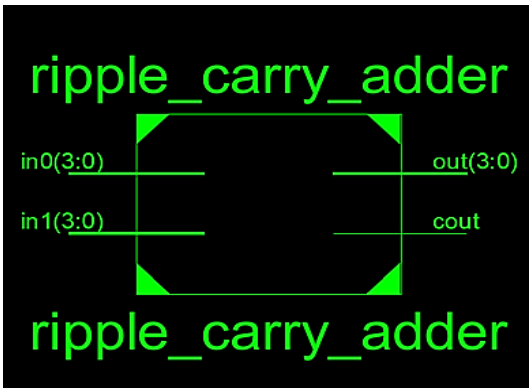

Figure 6: *Ripple Carry Adder*

Although the top level of RCA is equal, but the entire adder representation is altered as seen in Fig 6. Binary inputs 0 (3:0) and 1 (3:0) are used to drive the outputs in Fig 7, which are going to be (N-1 down to 0).

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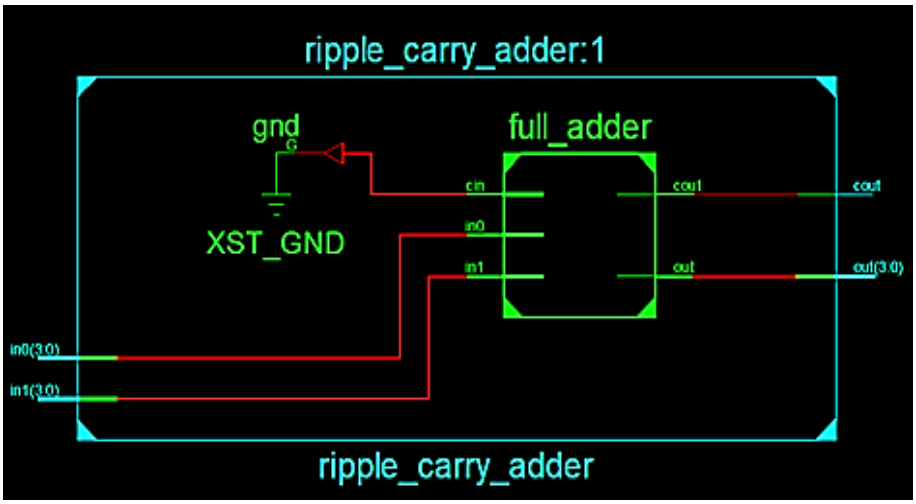

Figure 7: *Ripple Carry Adder*

This full adder optimization, which is the simple solution for RCA, aims to minimize the full adder's carry in and carry out delays. The combinational logic of the RCA circuit is used. It is applied to the addition of two binary values of length n. Its circuit requires n full adders in order to add two n-bit binary values. Another name for it is an n-bit parallel adder.

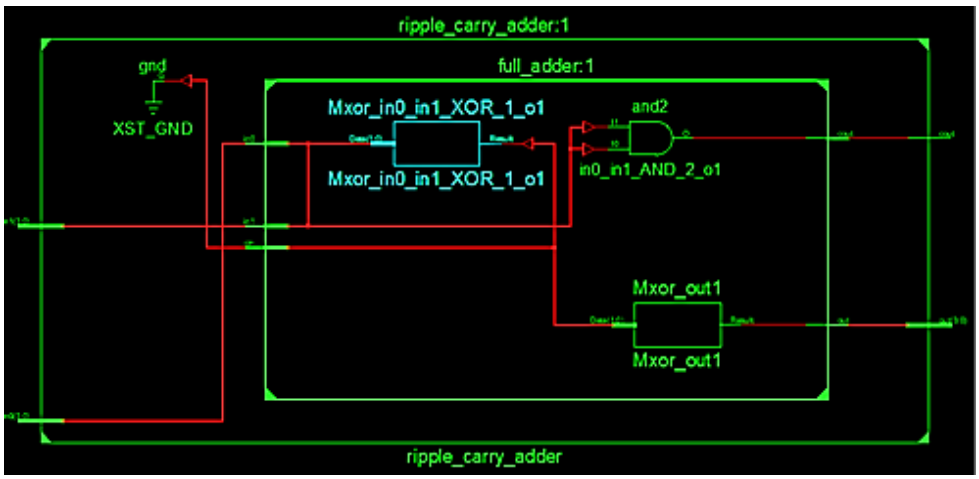

Figure 8: *Symmetric Diagram*

The symmetric XOR AND gate diagram is displayed in Fig 8.
When the codes are correctly simulated in Xilinx ISE Design Suite 13.4, the waveform that results is as follows.

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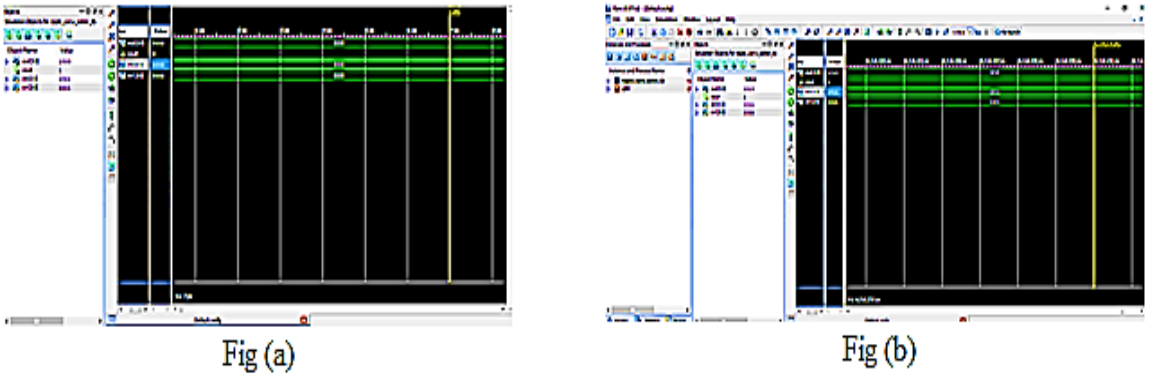

Figure 9: *Simulation Waveform of RCA*

5 Conclusion

This research presents a ripple carry propagate adder-based high-speed area-efficient technique. As long as a single module doesn't have more than one defect going at once, which detect many faults at once. The proposed RCA's area-power-delay product is enhanced. The recommended design outperformed the current designs in terms of efficiency and cost-effectiveness, according to the data. As a result, they will be efficiently applied in the design of increasingly intricate systems and circuits to enhance and optimize composite and intricate circuits.

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